APPLICATION NOTE

# Hybrid Analogue/DVB TV Receiver IFA1999 Demonstrator

## AN99061

Philips Semiconductors

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PHILIPS

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**Abstract**

This application note describes the implementation of a hybrid TV receiver capable of handling both analogue and digital transmissions with one tuner. During the transition phase from analogue towards full digital transmissions, these hybrid TV receivers are needed in the market.

The aimed market segment for the presented concept is called LMR-DTV. A “low” range digital source decoding part (designed as an “add-on”) is economicly combined (via a new designed interface) with a mid range analogue $110^{o}$, 16:9 TV receiver.

The receiver was build as a demonstrator and is part of the LMR-DTV system study of PS-SLE.

The analogue part is based on the TDA8885 version of the Philips Semiconductor one chip TV IC family, designed for the European market and thertefore not full RF multi standard. Via the tuner PAL-B/G-I-DK, SECAM-B/G-D/K-L-L1 is implemented. Via external inputs this is extended with NTSC-M, PAL-N,-M.

For the digital part, two channel decoding options are worked out: DVB-C and DVB-T. For the COFDM demodulator the VES9600 is used. The MPEG-2 source decoding part is implemented with the SAA7214 and SAA7215 as used for the Philips Semiconductors set-top box reference design STB5660.

With rewritten and adapted embedded software, the possibility for **one** user interface (all OSD/OSG generated by SAA7215) for both analogue and digital frondend modes is shown.

The full working hybrid TV receiver was build and demonstrated to external customers by PS-SLE at the Philips Semiconductor show held in Hotel Berlin during the IFA in august 1999.


Purchase of Philips $I^2C$ components conveys a license under the Philips $I^2C$ patent to use the components in the $I^2C$ system, provided the system conforms to the $I^2C$ specifications defined by Philips.

## APPLICATION NOTE

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## AN99061

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**Summary**

This application note describes the implementation of a hybrid TV receiver capable of handling both analogue and digital transmissions.

The analogue part is based on the TDA8885 version of the Philips Semiconductor one chip TV IC family. The receiver is designed for the European market and thertefore not full multi standard. Via the tuner PAL-B/G-I-DK, SECAM-B/G-D/K-L-L1 is implemented. Via external inputs this is extended with NTSC-M, PAL-N,-M.
For the audio part, the Philips multsitandard TV sound processor TDA9875A is used. The speakers are driven by the new TDA8946 sound amplifiers.

For the digital part, two channel decoding options are worked out: DVB-C and DVB-T. For the COFDM demodulator the VES9600 is used. The MPEG-2 source decoding part is implemented with the SAA7214 and SAA7215 as used for the Philips Semiconductors set-top box reference design STB5660.

The reception for both transmissions can be done via one tuner. The Philips CD1516 for analogue and digital cable transmissions and the TD1544 for analogue and digital terrestrial transmissions.

The used video amplifier is a TDA6108 and has a bandwidth of 9Mhz (100Vpp). No alignment at the board is necessary, it is done via IIC-bus.

The 200W power supply is build around the TEA1504 GreenChip SMPS controller. Vertical deflection is made with the new LVDMOS driver family TDA8359.

The deflection supports linear zoom in vertical AND horizontal direction (Philips patent), all geometry control for the Philips RealFlat picture tubes is present. The demo receiver is made with a 32 inch RealFlat tube.

The receiver is made modular and split in three parts:

1. A single layer large signal board

2. A double layer small signal board

3. A four layer digital board

With rewritten and adapted embedded software, the possibility for **one** user interface (all OSD/OSG generated by SAA7215) for both analogue and digital frondend modes is shown.
A short software user manual is described and also the known problem list.

This Application Note should be read together with the Application Note AN99062. On an A3 paper size the diagrams, layouts and bill of materials are presented.

The report is not complete yet. In a next version the system overview of the power supply &deflection, has to be added. The EMC part describes now the design aspects. Later on this chapter has to be expanded with the EMC measurements, results and improvement of the total system.

# Table of Contents

## 1. Introduction

This application note describes the implementation of a hybrid TV receiver capable of handling both analogue and digital transmissions. During the transition phase from analogue towards full digital transmissions, these hybrid TV receivers are needed in the market.

In order to enter the high volume market, the introduction price for these hybrid TV receivers must be kept as low as possible. This market segment is idented and named LMR-DTV (Low-end digital, Mid-Range analogue, Digital TeleVision). Several LMR-DTV concepts are made. In this report two implementation are described:

SLE3500 Multistandard Analogue reception combined with DVB-T
SLE3510 Multistandard Analogue reception combined with DVB-C

The work is done as part of a system study. One goal was to present a working model at the Philips Semiconductors show held in Hotel Berlin during IFA'99. Although the DVB-T hybrid is the most important design, within the available time frame the DVB-C hybrid was seen as the most successful candidate to show at IFA. During the project the VES9600 COFDM demodulator became available and the DVB-T combination was also made but with a separate VES9600 board. There was no redesign made with the VES9600 at the place of the DVB-C QAM demodulator. During the IFA the SLE3500 was presented with a via the Common Interface connector connected external VES9600 COFDM demodulator board.

This report must be read together with report AN99062 which contains the diagrams, layouts and bill of materials on an A3 paper size.
On these diagrams the SLE3510 concept is presented. The used DVB_C QAM demodulator is the outdated TDA8048 device, it will be replaced by VES1820.

The idea of the presented LMR-DTV receiver concept is that one can make a 50Hz Mid-End TV receiver chassis and design it in such way that **without a redesign** one can add a digital reception part to it. In this way it is not necessary to make a dedicated hybrid receiver design.

For this reason the whole receiver is divided into three boards:
1. Single layer large signal part.
2. Double layer small signal part.
3. Four layer digital reception part which is the optional add-on to make it a hybrid receiver.

The small signal analogue reception part is based on the TDA8885H version of the one chip TV IC family with development name BOCMA. It also contains the SAA55xx or 56xx micro controller (Painter)and a digital multistandard TV sound device (TDA9875AH) is used.
The digital reception part is based on the SAA7214 (MIPS) and SAA7215 (DIVA) MPEG2 source decoding family. To minimise our software effort in the design phase, the outdated SAA7214 is used. In industrial designs it should be replaced by the SAA7219.
The power supply is based on the new Green Chip SMPS control IC family TEA1504 and TEA1501 (Greeny). Vertical deflection is done with the new TDA8357 vertical driver. Audio amplifying is done by the new TDA894x family (TDA8946). The picture tube is driven with a TDA6108 video amplifier.

With rewritten and adapted embedded software, the possibility for **one** user interface (all OSD/OSG generated by SAA7215) for both analogue and digital frondend modes is implemented. Not **all** analogue OSD control menus are converted to SAA7215. For this demonstrator only the channel number and the volume bar are made equal for both analogue and digital fronden modes.

## 2. System Overview

This chapter describes the different building blocks of the hybrid TV receiver.

### 2.1 Design Specifications

The demonstration receiver is designed for the European market. It has the following characteristics:

- Quasi-Split Sound with single reference IF system
- Off-air reception for:
  SECAM-BG-DK-L-L1, PAL-BG-I-DK video standards
  5.5 and 6.5MHz FM mono sound standards, AM France mono, B/G-2CS, NICAM-I and BG stereo standards
  NOT: BTSC and Japanese FM to FM stereo
- NTSC-M and PAL-M-N playback via external inputs
- AV1: One full SCART with CVBS in & out, Audio left/right in & out, RGB in (or Y/C in AV1S)
- AV2: Second SCART with CVBS in & out, Audio left/right in & out
- AV2S: S-VHS Y/C Hosiden input (Y in parallel to AV2 CVBS)
- AV3 on front: in this demonstrator only available WITHOUT digital reception part, CVBS in, Audio Left/Right in
- AV3S on front: only available WITHOUT digital reception part, Y/C in (Y in parallel with AV3 CVBS in)
- Stereo headphone 3.5mm output jack connector on front
- Optional Dolby Surround Pro Logic decoding with extra small board
- YUV connector for optional extra picture improvements or a simple PIP application
- Deflection circuitry also prepared for Philips 50Hz real flat picture tube
- Deflection with linear vertical and horizontal zoom capabilities according to SLE patent
- 200W SMPS part, approx. 90W reserved for audio power
- Hybrid Analogue-Digital TV
- Optional Dolby Pro-logic decoding
- MPEG-2 Audio & Video
- PCMCIA Interface Slot

When the digital reception part is added the AV3/AV3S input is sacrificed and used for the video and audio output of the MPEG decoder. Now the next properties are added:

- DVB-C demodulation up to 256-QAM **or** DVB-T demodulation for COFDM-2k/8k (ETSI 300 744)
- MPEG2 source decoding
- Digital ENCoder (DENC) and ADC to convert back to PAL-CVBS-Y/C, RGB and Left/Right audio
- Digital audio SPDIF output
- RS232

## 2.2 Board Setup

The choice of this concept is to split the TV functions in three parts. The board set up is given below.

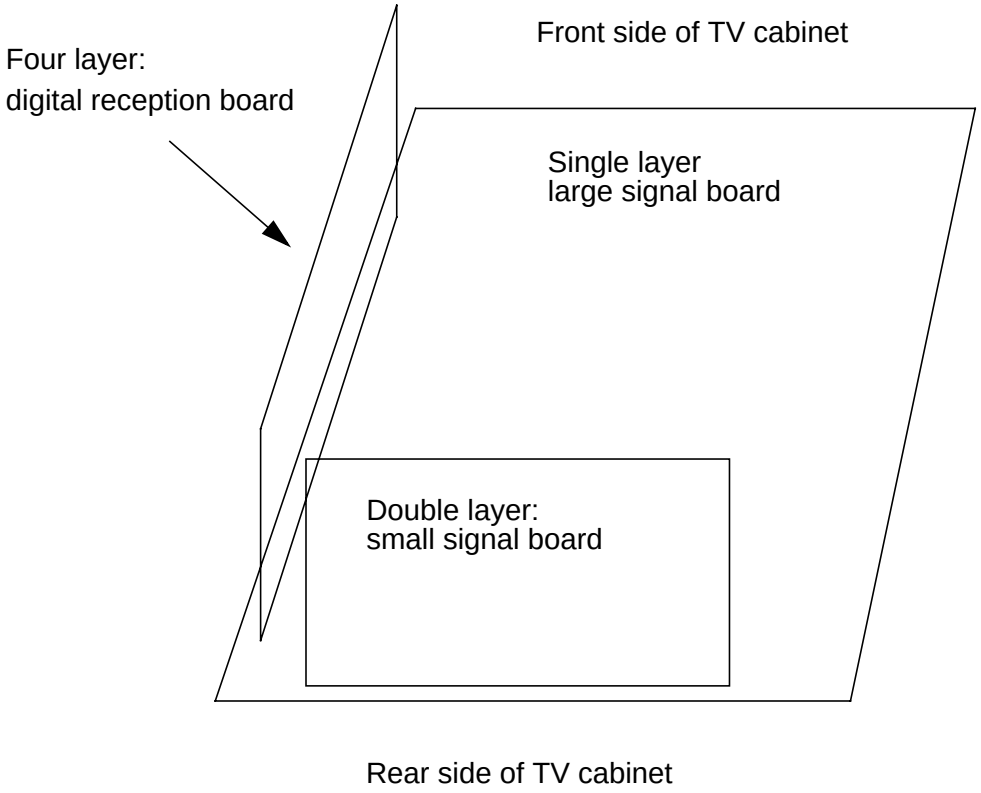



Fig.1 Board setup

The digital reception board is placed on the edge of the large signal board. Now when only the analogue TV receiver has to be produced, the large signal board needs no redesign. The only difference is that the connector row is not mounted, the large signal board will be smaller and the signal leads to the digital reception board are not routed. The rest remains the same. This is shown in the “Analogue and Digital Interface” paragraph. In this figure the red coloured (or light grey) parts are only needed for the digital add-on. The signal sequence in the connectors are chosen in such way that when the digital add-on is used the other connectors on the small signal board are not needed anymore. The signal sequence in the interface is also optimized for minimum signal crossings. This was needed specially for the small signal board which is in fact a single layer design due to the full copper bottom layer. The remaining crossings are made with isolated wire jumpers which can be replaced by SFR16 0Ω jumpers for factory production.

To make our engineering phase more flexible, the large signal part is splitted in two boards. Via the large and small signal interface board PR33441, we can use different power supply and deflection concepts. PR33441 is designed in such way that you can combine the layout of PR33441 and PR33341 to one board.

1. Large signal: the combination of PR33441 and PR33341
2. Small signal: PR33371
3. Digital part: PR33321

The board setup is shown on the next photo:

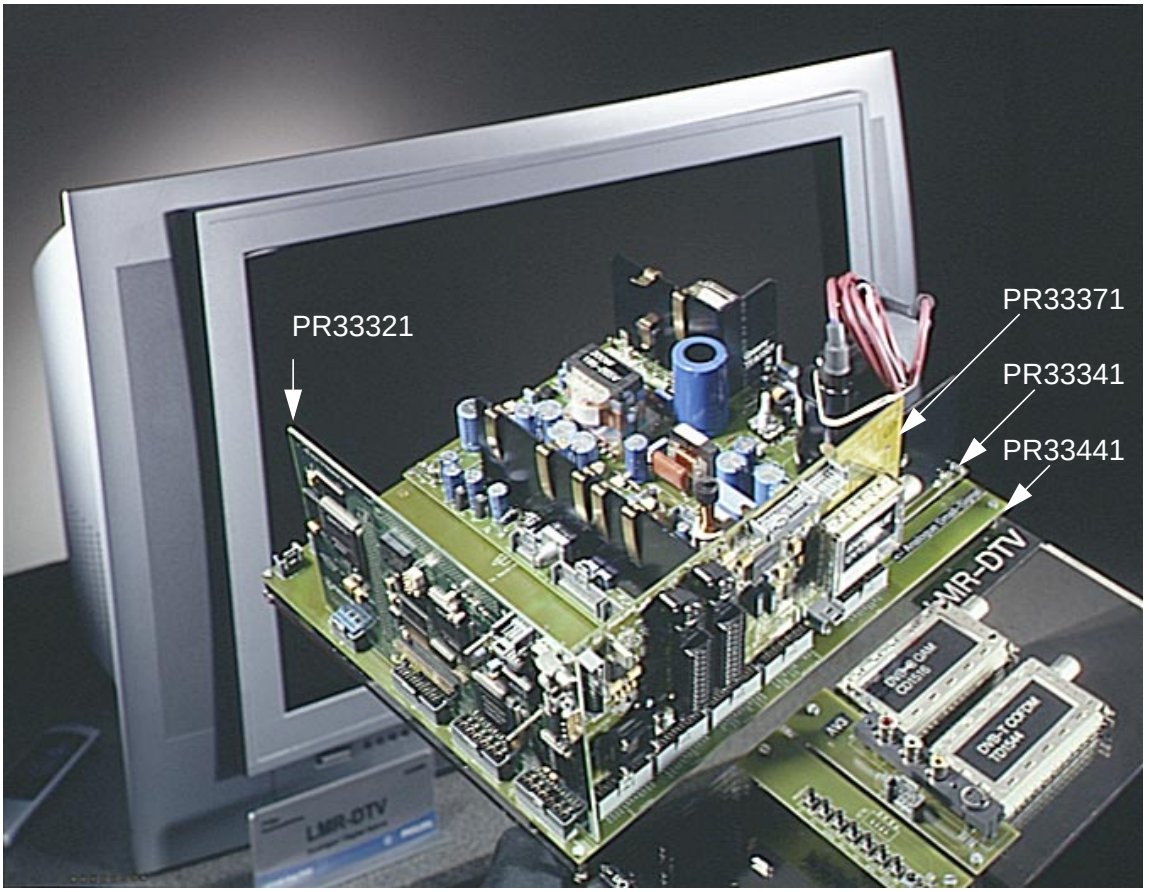
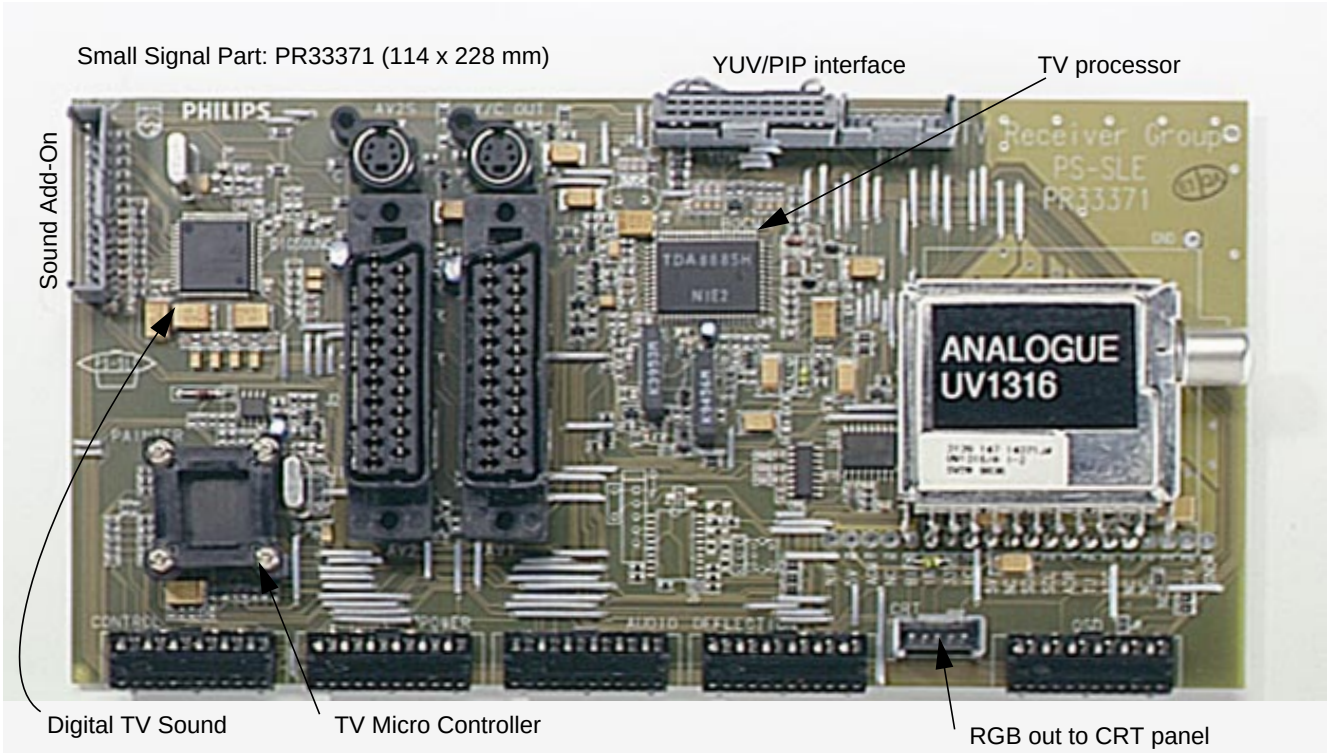



Fig.2 Total hardware fotograph

The demo receiver consist of four boards:

1. PR33441: Interface Board Large and Small Signal
2. PR33341: Large Signal Board (Switch Mode Power Supply & Deflection)
3. PR33371: Analogue Reception & Processing Board
4. PR33321: Digital Reception & Processing Board

Fig.3 .Small Signal Part & Digital Reception Part photographs




Digital Reception Part: PR33321 (125 x 206 mm)

NOTE: on the foto the VES9600 is not the actual device.
The new VES9600/R will almost be the same package as on the photo.

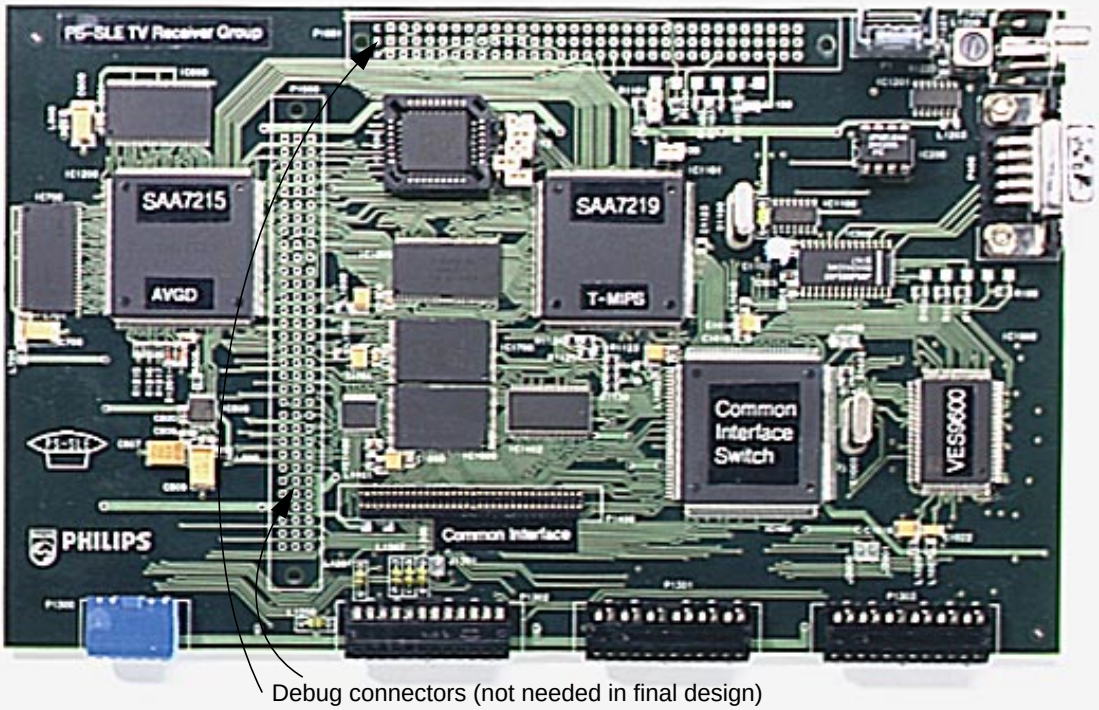


Fig.4 Large Signal Board: combination of PR33441 and PR33341 (total is 250 x 321 mm)


## 2.3 Design Considerations

The system is split in three parts. Large signal, small signal and optional digital reception part. Now several combinations can be designed without a redesign of the total.
If, for instance the small signal part needs to be redesigned for a newer chipset, the rest can be the same. This is also true for the digital reception part, it can be modified without changing the other boards.
To support this flexibility a well defined interface is used in the form of a row connectors to interface the small signal board via the large signal board towards the digital reception part.

Another option is to change the large signal part from 50Hz to 100Hz application. Now the small signal board chipset is modified and a 100Hz converter box has to be added. This can be positioned in parallel behind the small signal board. In this situation the digital reception part needs no adaption. This 100Hz hybrid concept is not worked out.

The small signal board is positioned at the rear side of the cabinet. The peripheral connectors are also placed on the small signal part. This approach is not conventional. In current designs the peripheral connectors are mounted on the large signal board. In the presented design a lot of wiring, between the

small signal part, were the signal switching is done, and the large signal board, is not needed. This saves a lot of long wiring and board space.

Compared to our previous mid-end concepts GTV2000 or GTV3000, which were presented during IFA in 1997, the board space is now reduced with approx. 50%. This is also due to the fact that all used ICs are now SMD packages.

The ICs on the small signal board are located in such way that the minimum track length is needed from and to the peripheral connectors. For this reason the SCARTS are located between the digital sound IC and the TV processor.
The peripheral connectors are also used to make a separation between the mainly analogue processing part (like tuner, IF, TV processor) and the digital signal processing part (digital TV sound processor and TV controller) for better EMC behaviour.

The demo receiver is designed for the European market. For this reason SCART connectors are mounted, but on the same location, in a redesign cinch connectors can be placed.

The IF part is not full multi standard, only the european standards are supported. In case of DVB-T the “analogue” UV1316 tuner is replaced by the TD1544 COFDM tuner. The small signal board is prepared for that. Now also a mixer IC TDA9829T must be used to mix down the IF 36.15MHz to low-IF 4.57MHz for the VES9600. For DVB-T an extra position on the PCB is reserved for a second COFDM SAW filter.
In case of DVB-C a CD1516 tuner is used but than the extra SAW is not needed.

For EMC reasons the tuner is placed at the right hand side when you view the chassis from the rear side of the cabinet. Now we have the shortest ground connection from tuner ground towards the mains entry cord where
the Y capacitors are grounded. For injected current immunity this was seen as the most successful approach. The consequence is that the tuner is also very close to the horizontal deflection. To prevent magnetic coupling between the large signal part and the small signal part, the small signal board has a full copperplane at the rear side. This copper plane is not used as a jumper layer, all used jumpers are isolated wire jumpers on the component side (in production they can be replaced by 0Ω SFR16 jumpers).

To keep the price as low as possible, the board space of the small signal part must be kept small. For all ICs SMD packages are chosen. On the photo’s the TV controller is mounted in a socket. This is only for the engineering phase. A metal mask programmed TV controller for production is soldered directly on the print.
First all SMD components are mounted, soldered by a reflow method. After that all leaded components and connectors are mounted which are flow soldered. In the presented setup the tuner must be mounted afterwards. We made not an industrial solution for this. Since conventional tuners have a straight connector outlet, they must be connected via a cable to an antenna entry mounted in the back cover of the cabinet.
If for EMC reasons the immunity for injected currents must be increased, this internal cable gives also the flexibility to apply a toroid inductor in this coax to avoid ground currents.

The digital reception board is positioned as far away as possible from the sensitive small signal IF part. To prevent magnetic coupling, the ICs on the digital reception part are mounted on the left side (seen from the overview photo position). The right side of this board is only a wire layer with some small SMD components. The two inner layers are full ground planes. This is different from the conventional 4 layer

setup were the inner layers are a ground plane combined with a power plane. The reason for this different approach is that with two inner ground planes the other two wire planes will have identical coupling to the inner layers. Another reason is that now with a relative small redesign effort a two layer version can be made. The two inner ground planes are taken out and the remaining wire layers are expanded with ground. Most likely the board space will increase a little but a two layer board is more cheap than four layers. This redesign is not done yet.

The large signal board is made with the new GreenChip SMPS controller. For low power stand-by mode an extra Greeny controller is reserved. The low voltage supplies for mainly the digital part are made with a small DC/DC convertor. The large signal board layout is made as compact as possible. Compared to our previous concept a 14% reduction on board space is achieved.

## 2.4 Analogue & Digital Interface

To support the separate functions (large signal - small signal - digital add-on, implemented as a three board setup) in an economically build receiver, a well defined (and stable) interface between the boards is needed.

In the next two pictures the overall block diagram and the analogue to digital interface are drawn.

The pin sequence of the connectors on the interface board are chosen in such way, that on the small signal board the minimum amount of crossings are needed. On this, in fact single layer board, crossings of leads, are made with wire jumpers.

To further optimize the pin sequence, iterative checks were done for:
- the minimum crossings on the (single) layer large signal board
- a short connection between small signal and deflection part
- a short connection of tuner and IF circuitry
- a direct ground connection from tuner ground to mains entry safety capacitors (for EMC)
- short connection of audio and video in- and outputs towards the audio and video switching devices
- a separation of sensitive analogue and radiating digital circuitry
- the possibility for YUV interface expansion slot and the room for such an add-on board
- the same for an audio feature extension add-on board
- minimise the potential crosstalk between signals

These considerations eventual leaded to the presented location and orientation of the IC’s and other components, in fact the layout of all three boards are related to the pin sequence in the interface connectors.

Another design goal was that the small and large signal interface connector can be used for both the hybrid and analogue only version. For this reason the signals which are needed for analogue are located in the centre of the connector row. The signals needed for hybrid are chosen at the begin and end of the connector row, for analogue only they can be omitted and a smaller connector can be used.

## 2.5 Block diagrams

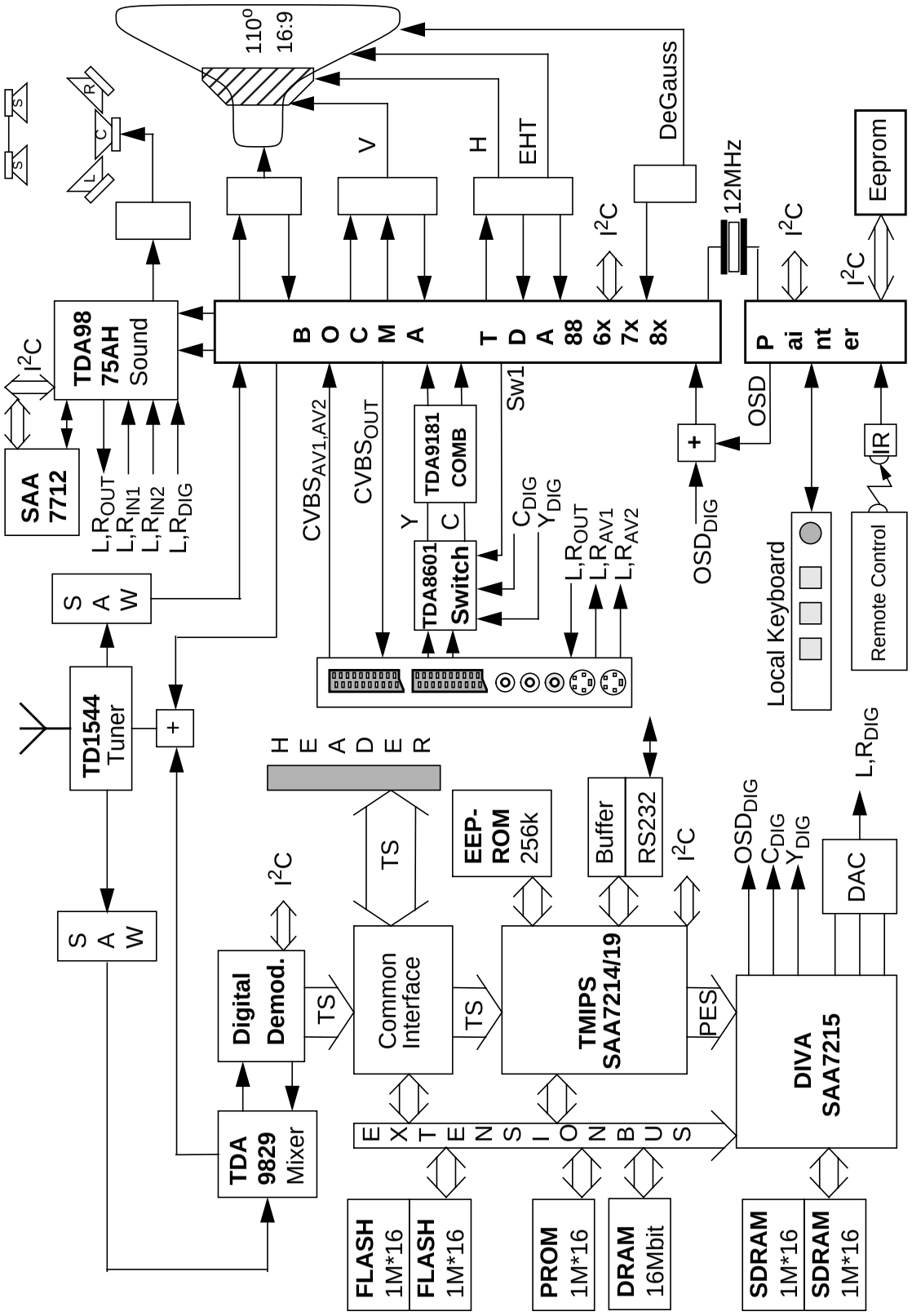



Fig.5 Overall Block diagram

### 2.5.1 Analogue & Digital Interface Board

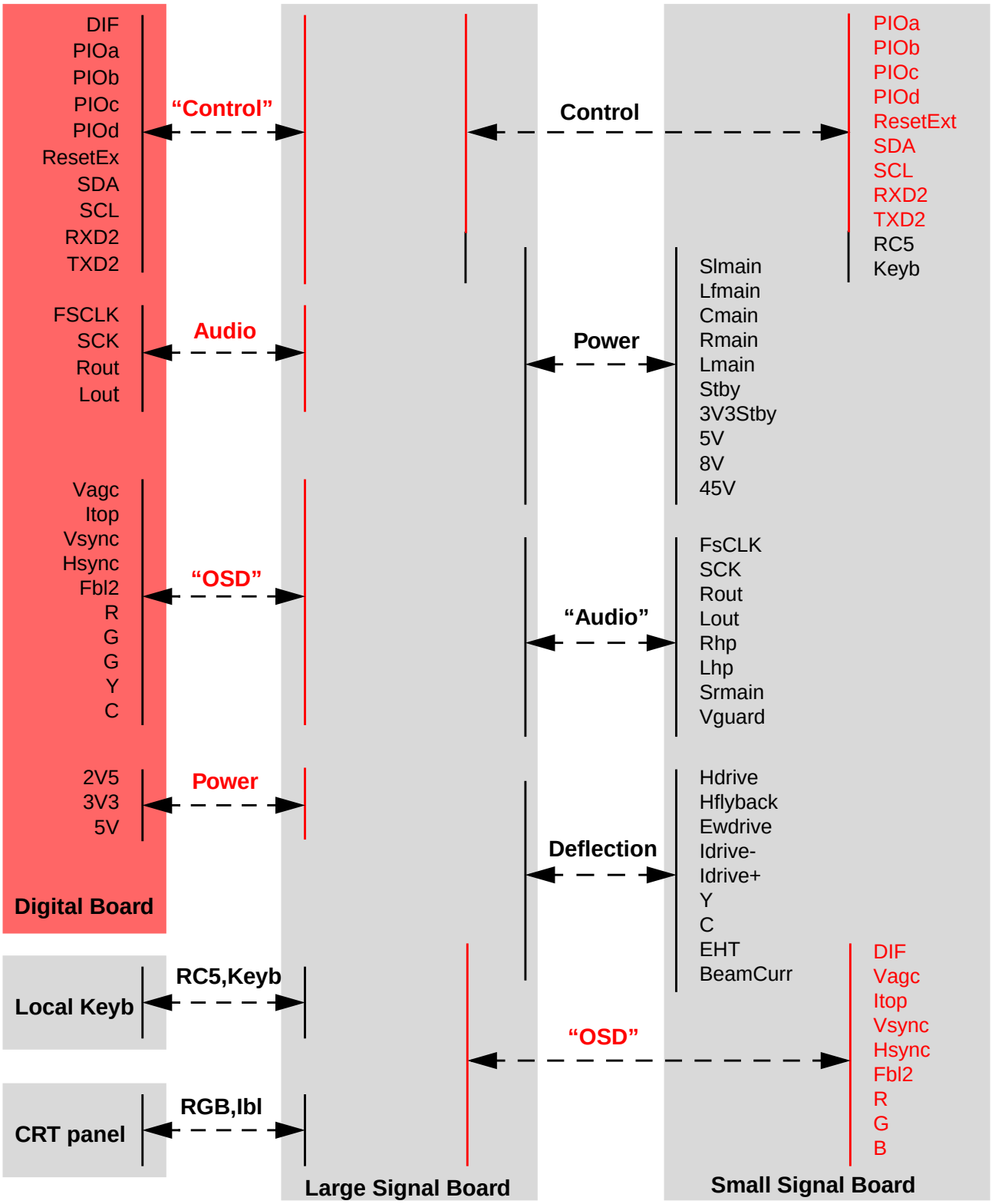



Fig.6 Analogue & Digital Interface

### 2.5.2 Analogue Reception Part

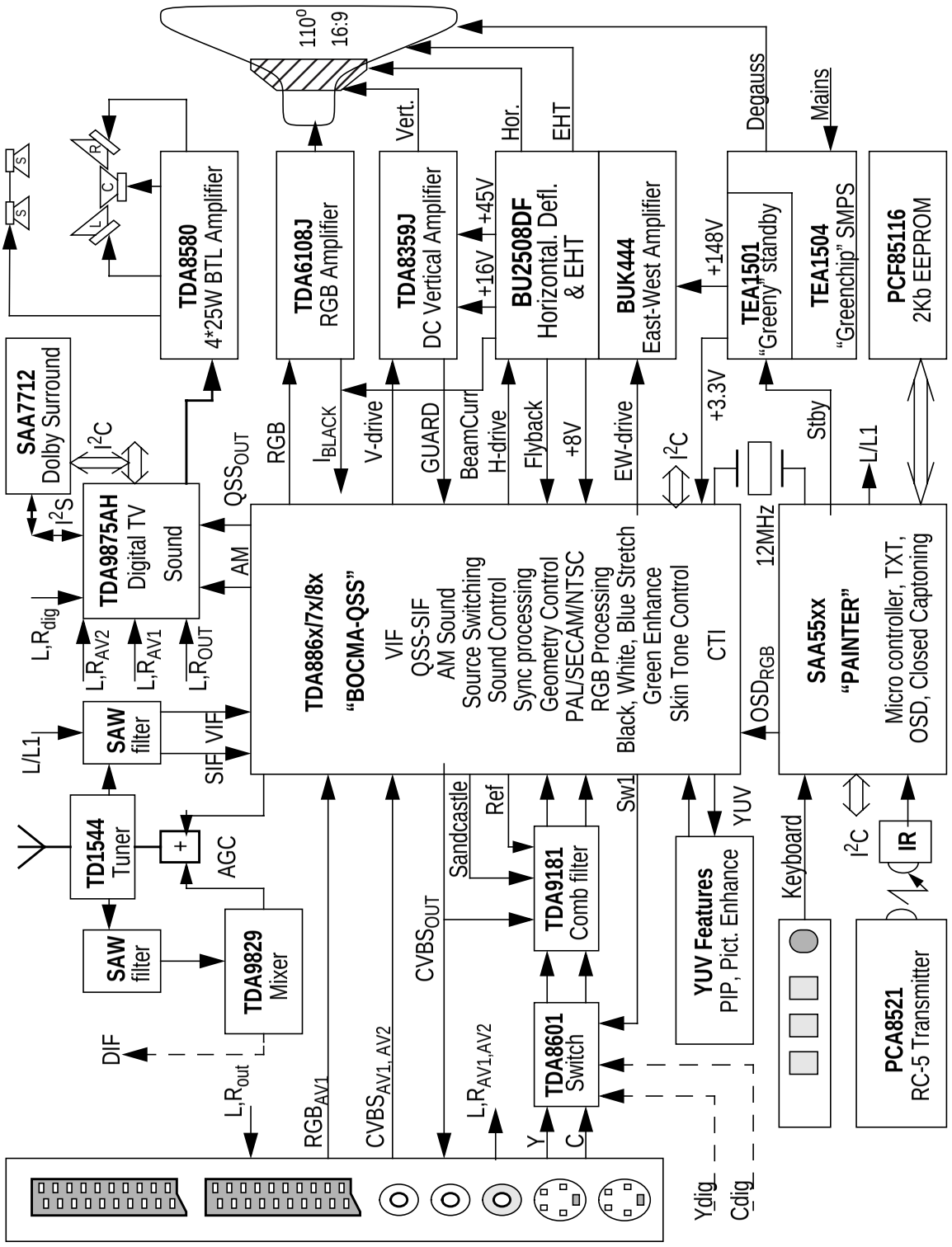



Fig.7 Analogue Reception Part: Block diagram

### 2.5.3 Digital Reception Part

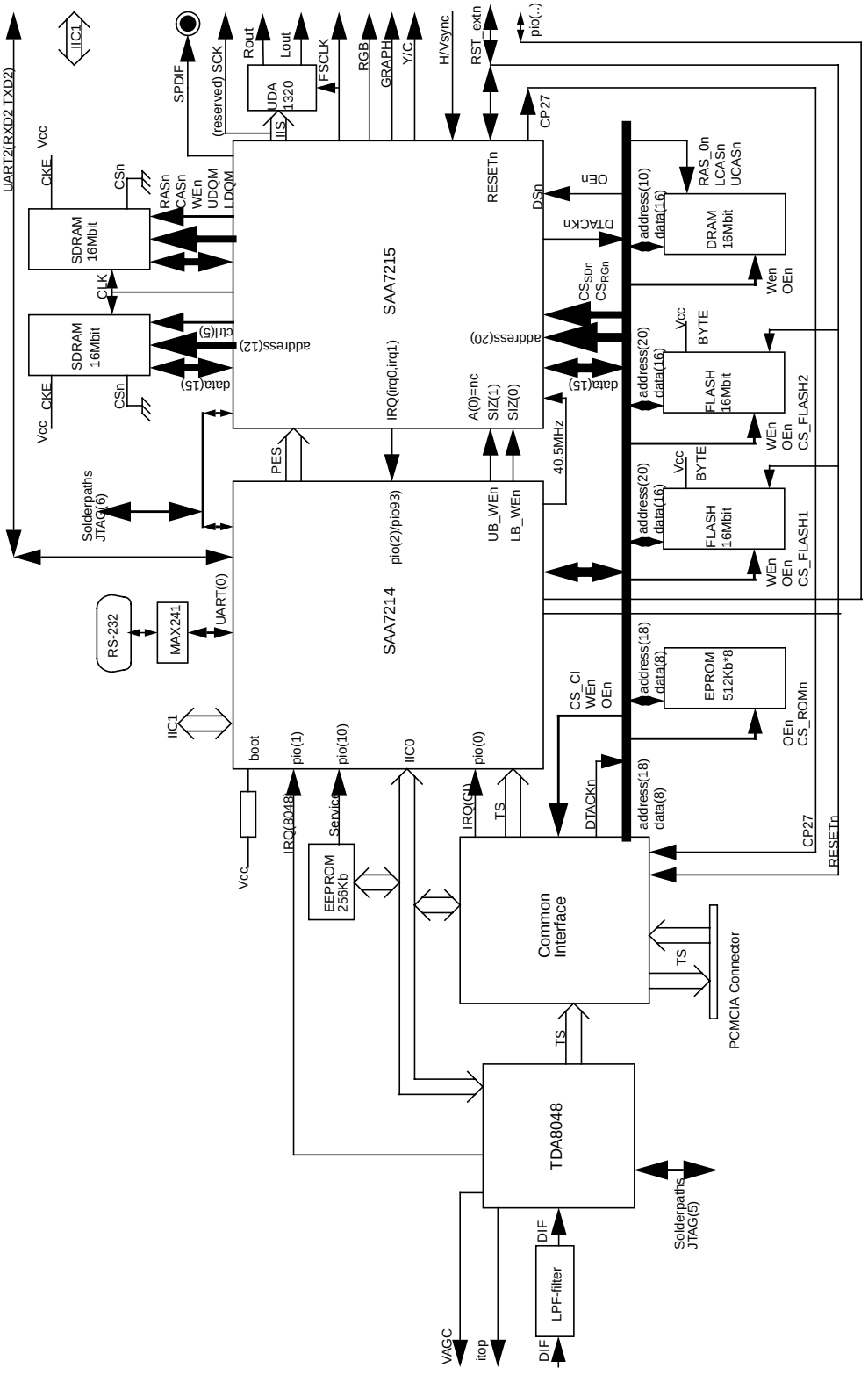



Fig.8 Digital Reception Part: Block diagram

### 2.5.4 Power Supply

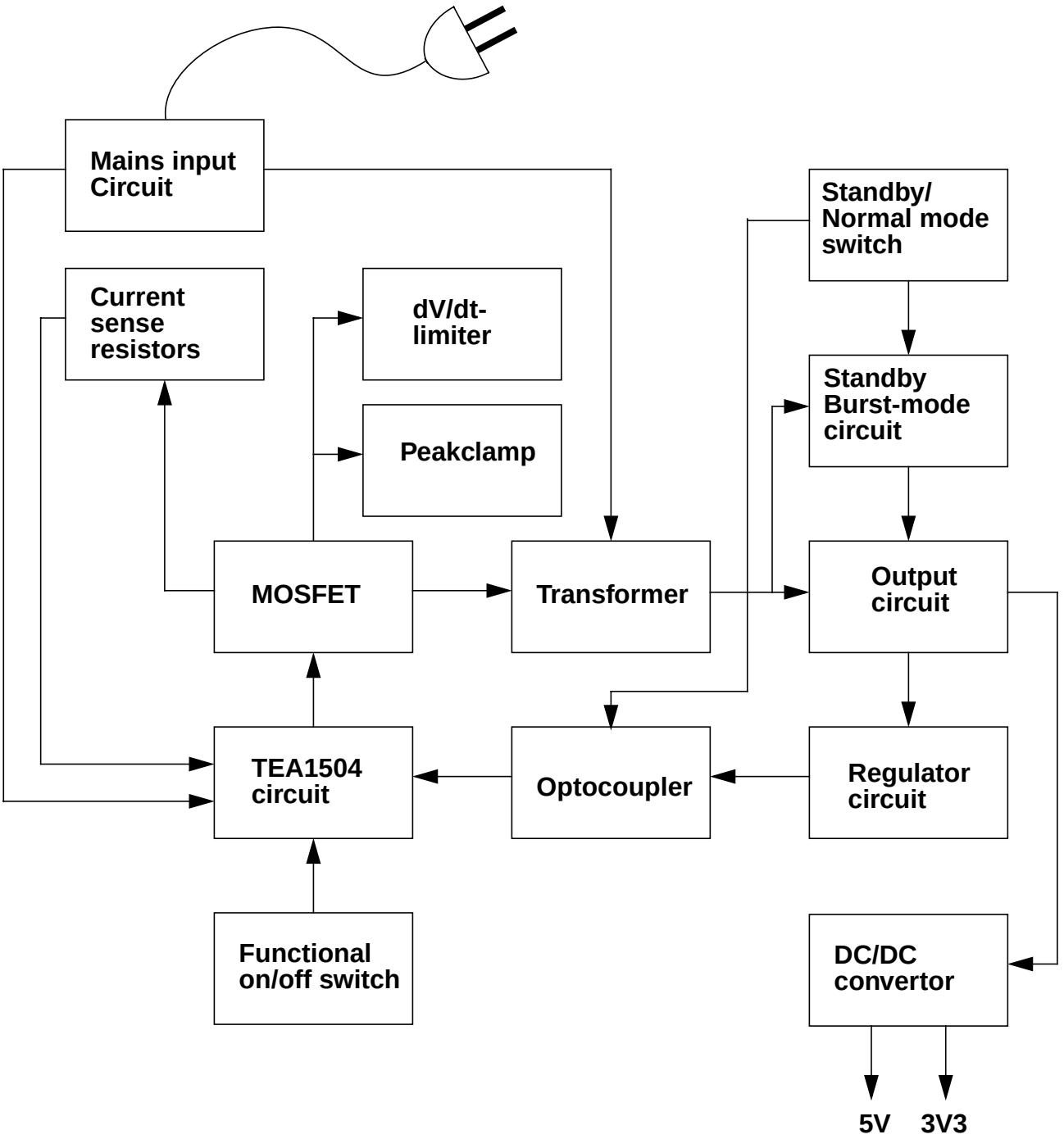



Fig.9 Power Supply Part: Block diagram

## 3. Analogue Reception Part

The analogue reception part is a separate board containing ALL the small signal functions for a mid-range TV receiver including tuner, peripheral connectors (two SCARTS, one input and one output SVHS connector), multistandard digital sound, comb filter and TV-controller. The core IC is an OneChip TV processor TDA8885 with development name BOCMA (Bimos One Chip for Mid-end Applications). This device covers all the processing from IF-in or external baseband inputs to RGB-out for a picture tube including the horizontal and vertical deflection control signals.

The tuner & IF part is designed in such way that different applications and/or TV receivers can be implemented on the same board. The different versions are made with different component settings and/or solder jumpers.

The target of this concept is that with one board design, two different types of receivers can be made:

1. Analogue Mid-Range TV set
2. Mixed digital/analogue hybrid TV set (indicated as LMR-DTV)

Via connectors extra functions can optional be added, like Dolby Pro Logic decoding and a simple PIP application. The sound add-on connector is prepared for a six channel audio decoding (like AC3) option. A YUV connector is present for additional picture improvements.

A lot of effort is put in the definition of an interface between the “analogue board”, the “large signal board” and the “digital board”. This interface is chosen in such way that future developments can be implemented (to a certain extend), like Scan Velocity Modulation, multi channel audio reproduction and direct digital interfacing of audio.

### 3.1 Tuner & IF Part

The concept is prepared for basically three types of tuners:

1. analogue tuners like UV1316
2. DVB-C tuners like CD1516
3. DVB-T tuners like TD1544

#### 3.1.1 Analogue only reception

For analogue reception an UV1316 can be used. This is a conventional three band PLL tuner with an IF frequency of 38.9MHz. The target of this reference design is to cover the European markets. For that reason the SAW filter application is not made full multi standard. The mid-end TV-processor TDA8885 has a quasi split sound with single reference IF-PLL demodulator. For the video SAW filter a type with double nyquist slopes was chosen; K3953M. For sound a switchable bandpass SAW filter is used; K9456M. This combination covers the standards B/G, I, D/K, L and L’. The sound bandpass filter is switched with the SW02 general output pin 60 of the TDA8885.

**TABLE 1 SAW filter switching**

| SW02 (pin 60) | Standard |
|---|---|
| 0 | L’ |
| 1 | B/G, I, D/K, L |

The BOCMA has an integrated group delay compensation. Now a multistandard SAW filter without group delay can be used and in case of B/G the internal B/G group delay is activated (bit GD).

With a different SAW filter choice other standards can be supported. An NTSC receiver can be made with e.g. an UV1336 tuner but than the SCART connectors need to be replaced by cinch connectors. The mounting of cinch connectors is not implemented in this board design.

### 3.1.2 Analogue and digital reception (DVB-C or DVB-T)

In case of an hybrid receiver the CD1516 or TD1544 is ALSO used for the analogue reception, there is NO need to use two tuners.

The application of a DVB-S front-end is not supported in this design. For a DVB-S hybrid receiver a different board setup with two tuners must be used (or a hybrid analogue terrestrial and satellite tuner must be developed).

In the IF part on the analogue board, the provision is made to have two different time constants for the tuner AGC. The time constant can separately be optimised for analogue and digital reception mode. Via a pushpull output port on the TDA8885 (pin 22, SW1) the analogue Aagc (SW1=0) or the digital Dagc (SW1=1) time constant is activated. The Philips 1300 (and 1500) tuner series must be alined to a maximum output level of 105dB$\mu V_{rms}$ which is equal to 500m$V_{pp}$ measured at an input level of 5mV or more via the tuner take over point settings in the BOCMA.

#### 3.1.2.1 Hybrid IF part DVB-C

In the preparation phase of this hybrid reference design, the DVB-C QAM demodulator TDA8048 was on the IC roadmap. This product will now be replaced by the VES1820 and derivatives of it. For more information of TDA8048 see ref. [1]. The application of VES1820 or successors for this reference design are not implemented yet, it is just the replacement of TDA8048 by another device. The board setup and design will not change.

In case of DVB-C the Siemens/Matsushita SAW filter type X6966M is used. In that case the tuner IF frequency must be set to 36.15MHz.

At the IF output of the tuner a down convertor TDA9829 is used to mix down IF to low-IF. After a low-pass filtering the ADC at the input of TDA8048 can convert the QAM carrier to the digital domain where it is further processed to a transport stream output format.

The TDA8048 controls the gain of the IF amplifier inside the TDA9829. The TDA9829 controls the tuner gain. The total gain is controlled by the TDA8048 in such way that the input voltage at the low-IF ADC TDA8048 input is constant. It is a closed loop feedback system. No adjustment is needed.

#### 3.1.2.2 Hybrid IF part DVB-T

The COFDM demodulator VES9600 IF application is basically the same as the DVB-C demodulator. Again a down convertor TDA9829 is used to make a low-IF signal which is fed to the VES9600. The successor VES9600/R will also support direct IF input at 36.15MHz, now the down conversion is not needed anymore.

## 3.2 OneChip TV Part: TDA8885 (BOCMA)

The heart of the analogue part of the receiver is the TDA8885 which is a member of the TDA886X/7X/8X one chip TV processor family.

Common features of this IC family are:

- Multi-standard vision IF circuit with an alignment free PLL demodulator
- Internal time-constant for the IF-AGC circuit
- Integrated switchable sound trap and group delay correction for the demodulated CVBS signal
- Flexible source selection with CVBS switch and a Y(CVBS)/C input for comb filter
- Integrated chrominance trap circuit
- Integrated luminance delay
- Integrated chroma band-pass filter with switchable centre frequency
- Colour decoder which needs one 12 MHz reference crystal for all standards
- Blanking of the ‘helper signal’ for PAL$^{PLUS}$ and EDTV-2.
- Several picture improvements features
- Internal base-band delay line
- YUV interface
- Linear RGB input and fast blanking
- RGB control with CCC, white point and black level off-set adjustment
- Adjustable peak white limiting circuit
- Half-tone possibility
- Blue back option
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages for improved geometry
- Low-power start-up for horizontal drive circuit
- IIC bus control of various functions

### 3.2.1 BOCMA IF part

The BOCMA has an alignment free IF-PLL demodulator. The fully integrated oscillator is automatically calibrated, using the 12MHz crystal as a frequency reference. The IF frequency is simply set by I$^2$C-bus bits **IFA**, **IFB** and **IFC**. All commonly used frequencies can be chosen. Depending on the SAW filter, 33.40 or 33.90MHz for SECAM-L1 in France, 38.00MHz for China, 38.90 for Europe, 45.75 for America and 58.75 MHz for Japan. The AFC information is available via I$^2$C-bus bits **AFA**, **AFB**. Embedded software uses this for tuner frequency tracking (= “automatic following”, AFC). The AFC window is typically 100kHz wide. This value is chosen higher than the 62.5 kHz tuning steps of a PLL tuner, to prevent the AFC loop from continuously adapting the tuning frequency. The internal AFC

accuracy is much less than 62.5kHz. For high speed search-tuning algorithms, the AFC window can be widened to approx. 300kHz via bit **AFW**=1.
Bit **STM** reduces the coincidence detector sensitivity (status bit **SL**). This bit can be used during search tuning to skip very weak signals.

Independent of video contents (detection is before video demodulation), the IF-PLL lock status can be read via bit **LOCK**.

The IF-PLL loopfilter is an external lead-lag RC filter. The described component values are optimised for the best demodulator performance in “normal” conditions. To partially cover non standard transmissions, e.g. excessive phase or frequency modulation of the picture carrier, via bit **FFI** the IF-PLL control speed can be increased. To further optimize the IF-PLL performance (e.g. to have the optimal step response for a 2T pulse for a certain SAW filter application, or have the minimum video to sound crosstalk), the DC-offset can be minimised via the **Offset** control bits. This extra alignment is only for those applications were this better quality is covered with a higher set price. For standard applications the center setting is recommended.

When switched to an external source, potential crosstalk of noise from the internal frontend (when tuner is not tuned), to the external signal can be reduced via bit **IFS**. This bit reduces the IF gain with 20dB.

The signal to noise ratio of the selected video can be read via bits **SN1, SN0**. This information can e.g. be used in a channel autostore, channels are stored in the order of S/N ratios.

Another status bit is **AGC**, it reflects whether the tuner gain control output is active or not. The point of tuner gain reduction can be set via **TOP** (tuner take over point) bits. The Philips 1300 (and 1500) tuner series must be alined to a maximum output level of 105dBµ$V_{rms}$ which is equal to 500m$V_{pp}$ measured at an input level of 5mV or more.

The IF AGC time constant is in the BOCMA integrated and made switchable. With previous IC versions an external IF-AGC capacitor was used. The standard value was 2µ2F which is now equivalent to the “norm” mode. The IF AGC speed can be adjusted with **AGC1, AGC0** bits.

**TABLE 2 IF AGC speed settings**

| AGC1 | AGC0 | AGC speed | Equiv cap. value | Function |
|---|---|---|---|---|
| 0 | 0 | 0.7 x norm | 3.1µF | slow AGC, reserved for special field conditions |
| 0 | 1 | norm | 2.2µF | normal recommended setting, optimal for both positive and negative modulation |
| 1 | 0 | 2 x norm | 1.1µF | faster AGC for negative modulation as to improve airplane flutter performance |
| 1 | 1 | 4 x norm | 0.5µF | fastest AGC for negative modulation as to further improve airplane flutter performance |

The BOCMA is available in FM-mono intercarrier and in QSS-SR versions. For this receiver the TDA8885 QSS with single reference is used. This IF concept has a better sound performance than intercarrier mode. For the French AM sound system the integrated AM demodulator of the BOCMA is used. On a separate pin the sound carriers are available. Baseband AM out and SIF output signals are routed to the TDA9875A sound device for further processing.

### 3.2.2 Colour decoding

The decoder frequencies of the various standards are obtained from an internal clock generator which is synchronized by an external 12 MHz crystal. Settings are made via IIC. 12MHz was chosen to match the reference frequency of conventional TV micro controllers. Now one crystal can be used for both TDA886x/7x/8x BOCMA as for SAA55xx/56xx Painter devices. Two types of applications are possible:

1. Painter has the crystal, being the clock master for the BOCMA slave.
2. Bocma has the crystal and Painter is slaved.

In both situations the master device xtal output pin is connected via a series capacitor of 33pF to the slave device xtal input pin. The slave xtal output pin is left open. Attention should be paid to the layout of this track. Keep this track as short as possible, avoid crosstalk from other surrounding tracks or elements! If these conditions can not be implemented, reconsider a two crystal application.

If the BOCMA is used as the clock master, the low-power start-up pin must be used and connected to a standby voltage supply between 3 and 5.5Volt (5mA current consumption). Now the BOCMA device has a continues operating clock oscillator which is needed for the micro controller.

In all cases the used BOCMA crystal must have a low frequency tolerance and stability for a proper colour catching range. A suitable crystal is the Philips/SaRoNix 9922 520 00169 in a conventional HC-49/U13 package ($\Delta F_n$=30ppm).

### 3.2.3 YUV interface

A YUV interface is placed at the PCB. An application with histo booster (TDA9171) or a PIP application with e.g. SAB908X can be made.

### 3.2.4 Picture improvements

In the BOCMA various picture improvements features are integrated and can be controlled via IIC. In the embedded demo software for this receiver, most of the features can be controlled in the “Feature Menu”. For production the setmaker can choose for no features, subsets or all features active to make a model range with the same chassis. Another option is to combine features to picture settings with names, e.g. “Bright”, “Warm” etc. The features are shortly described in the next sub paragraphs.

#### 3.2.4.1 Video dependent coring

This is related to the peaking feature. The drawback of a peaking circuit is that noise in the video becomes more visible due to the peaking. Now the coring can be activated. Only in the low-light parts of the screen the noise is effectively reduced while still having maximum peaking in the bright parts of the picture. Three coring settings (and off) can be chosen with bits **COR1, COR0**.

#### 3.2.4.2 Colour transient improvement (CTI)

CTI decreases the rise and fall times of the colour difference signals. The colour transitions look more sharp. Bit **CTI** switches the function on and off.

#### 3.2.4.3 Dynamic skin control

Skin tones are very sensitive for hue errors, because we have an absolute feeling for skin tones. The goal is to make sure that skin tones are put at a correct colour. The dynamic skin tone correction circuit achieves this goal by instantaneously and locally changing the hue of those colours which are located in the area in the UV plane that matches skin tones. The correction is dependent on luminance, saturation and distance to the preferred axis and can be done towards two different angles. Depending on which part of the world there is a preferred skin tone. For example the 117 degrees angle can be the preferred skin tone in Asia where as in the USA and Europe the 123 degrees may be preferred. The preferred angle can be chosen via bit **DSA,** the correction range is 45 degrees. The function can be switched on and off with bit **DS**.

#### 3.2.4.4 Green enhancement

Green enhancement is intended to shift low saturated green colours towards more saturated green colours. This shift is achieved by instantaneously and locally changing those colours which are located in the area in the UV plane that matches low saturated green. Green enhancement is switched on and off via bit **GRE**.

#### 3.2.4.5 White stretch

White stretch adapts the transfer characteristic of the luminance amplifier in a non-linear way dependent on the picture content. It introduces additional overall gain for increased light production. For bright pictures the stretching is not active. Without increasing the brightness (black remains black) more details are visible in the darker parts of the picture. Via bits **WS1, WS0** three levels (and off) can be set.

#### 3.2.4.6 Black stretch

Black stretch corrects the black level for incoming video signals which have a deviation between the black level and the blanking level (back porch). This results in a maximum of visible details over the whole range of luminance. Bit **BKS** switches on and off.

#### 3.2.4.7 Blue stretch

Blue stretch is intended to shift colours near “white” with sufficient contrast values towards more blueish coloured white. A more sharp impression of the picture is percepted. The shift is accomplished by an offset at the RGB part of the BOCMA. Bit **BLS** switches on and off.

### 3.2.5 RGB outputs & CRT board

The RGB outputs of the BOCMA are connected to the CRT board via three small series resistors. The cable from the small signal board to the CRT-board also contains the ground connection of the video amplifier.
The BOCMA contains a two point continuous cathode calibration circuit (CCC) which stabilises the black level (offset) as well as the cathode drive level (gain) of each gun of the CRT sequentially and independently on alternating fields. It is a timed DC controlled feedback loop.
On the RGB outputs at the start of every field reference pulses are generated. Via the video amplifiers this leads to a certain CRT cathode current which is fed back to the black current input of the BOCMA.

In one field a current reference of 8µA is used, in the next field a value of 20µA is used. From the result of these pulses information of the CRT black level AND the amount of gain in the RGB path is generated. The black level of the BOCMA RGB outputs is adapted to the CRT black level and via the **CL** bits the drive level is set. Note that with this two point loop the video amplifier gain has NO effect on the CRT drive level anymore!
The black current feed-back line is the most sensitive part of the loop. For this reason some precautions have to be taken to avoid instability. If a flatcable is used (most of the cases) avoid crosstalk and separate the RGB wires (CCC-loop output) with the ground wire from the black current info wire (CCC-loop input). The preferred order is: BLKIN, GND, R, G, B.
A second precaution is to apply some filtering on the black current feed-back signal. In the design a capacitor (330pF) to ground (ground this capacitor to the “guard ground ring” if applicable), connected to the black current feed-back line coming from the CRT is used. From this point a series resistor (10kΩ) routes CCC info to the pin 30 of the TDA8885H. In this way all the black level info return current from theTDA6108 is first integrated (=low-pass filtered) and partial converted to a voltage by the capacitor. The series resistor converts the voltage back to current info.
On the CRT board a TDA6108 triple video amplifier with black current output is used. This device has a fixed gain of 51. To reduce the gain to approximately 45, three series resistors have been added directly at the RGB inputs of the TDA6108 (to prevent additional low-pass filtering due to the series resistor and the parasitic capacitance of a long RGB to CRT cable).
The gain of 45 is needed to obtain a more robust operating black current loop for a large variety of picture tubes. For the same drive level (which is measured via the black current loop and therefore can be controlled in the BOCMA via the **CL** bits) and a reduced video amplifier gain, the video input voltage is increased. In this way a better signal to disturbance ratio for the RGB signals is obtained.

The outputs of the video amplifiers are connected to the picture tube via special flash-proof resistors. All tube electrodes, not connected to ground, contain a spark-gap connected to the aqua-dag ground. The focus spark-gap is integrated in the tube socket connector. The aqua-dag ground is connected to the ground of the line transformer. This configuration has been selected to keep flash-over-currents in a loop as small as possible.

## 3.3 Comb filter

The TDA9181 is a multistandard PAL, PAL-M, PAL-N and NTSC comb filter IC with internal delay lines, filter, clock control, synchronization and signal switching. The application diagram is given below.

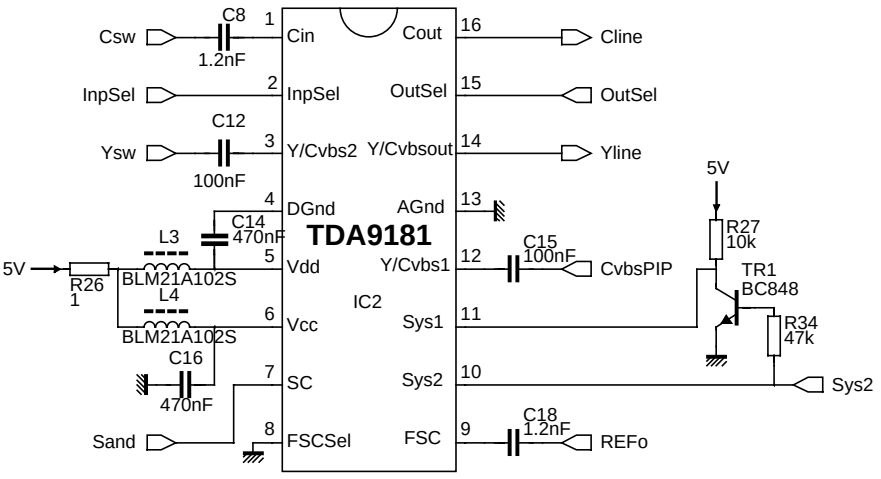



Fig.9 Comb filter application diagram

The Y/CVBS inputs are clamped by means of an internally generated clamp pulse which is derived from the sandcastle input (Sand).
The input switch (InpSel) determines which input signal passes through a low pass filter.
A colour subcarrier frequency signal (REFo) from the BOCMA is coupled via an external capacitor to the TDA9181.
The supply lines are filtered with series coils, a good ground plane under the IC is important as well as short decoupling.

The system switches (Sys1 and Sys2) determine which colour standard is used. For this Europe only receiver just two colour standards are implemented (PAL and NTSC) with one sys line (Sys2) which is controlled by the TV micro controller (Painter). If PAL-M and PAL-N has to be supported a second sys line is needed. The comb filter system truth table is given below.

**TABLE 3 Comb filter colour standards**

| SYS1 | SYS2 | Colour Standard |
|---|---|---|
| 0 | 0 | PAL-M |
| 0 | 1 | PAL |
| 1 | 0 | NTSC-M |
| 1 | 1 | PAL-N |

The internal comb filter block diagram is given below.

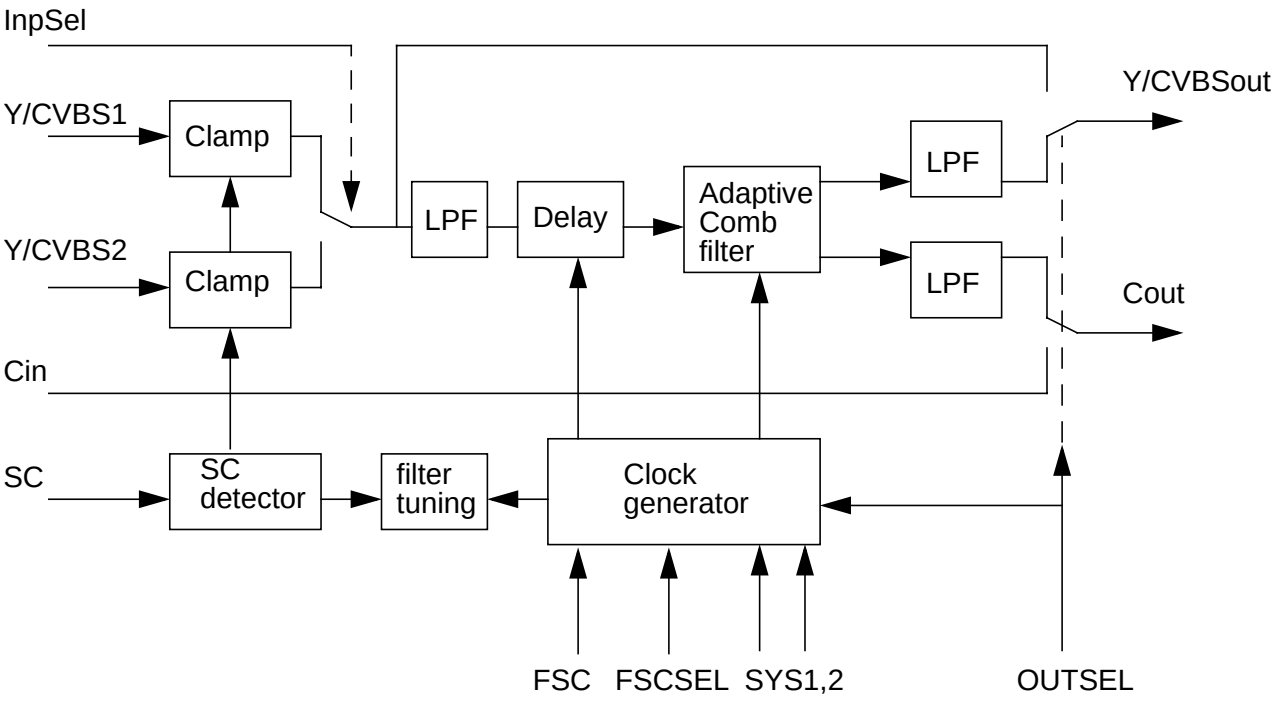



Fig.10 Internal comb filter block diagram

The output switch (OutSel) is not used in this application, the pin must be left open, now the pin is pulled-low by the comb filter (comb filter on condition). Note that the pull-up resistor at the Painter side is removed! The FSC (f subcarrier) is the REF output from the BOCMA, this signal is a sinewave with

the actual subcarrier frequency. FSCSEL is not used and forced low (REF=1 x $f_{sc}$). If FSCSEL is high you can apply a 2 x $f_{sc}$ frequency signal to FSC. When there is no REF signal coming from the BOCMA, or the comb filter can not lock to it, the comb filter switches itself in the bypass mode. In the BOCMA the REF output can be switched off via IIC (bits **CMB0, CMB1**). In this way the comb filter is switched on and off.

### 3.4 Peri & Switching

Without the digital add-on, source switching is possible between front-end, AV1(CVBS or RGB), AV2(CVBS or Y/C), AV2-S, AV3 and AV3S (note: AV2S and AV3S is not supported by the current software). Source switching is done directly with IIC in the BOCMA or indirectly via a BOCMA output pin SW1 which controls an external switching IC (TDA8601). For SVHS recording a Y/C output is made available (Yout, Cout).

When the digital add-on is used, AV3(S) is sacrificed and now used as the input for the digital reception part. The next diagram shows the peri switching.

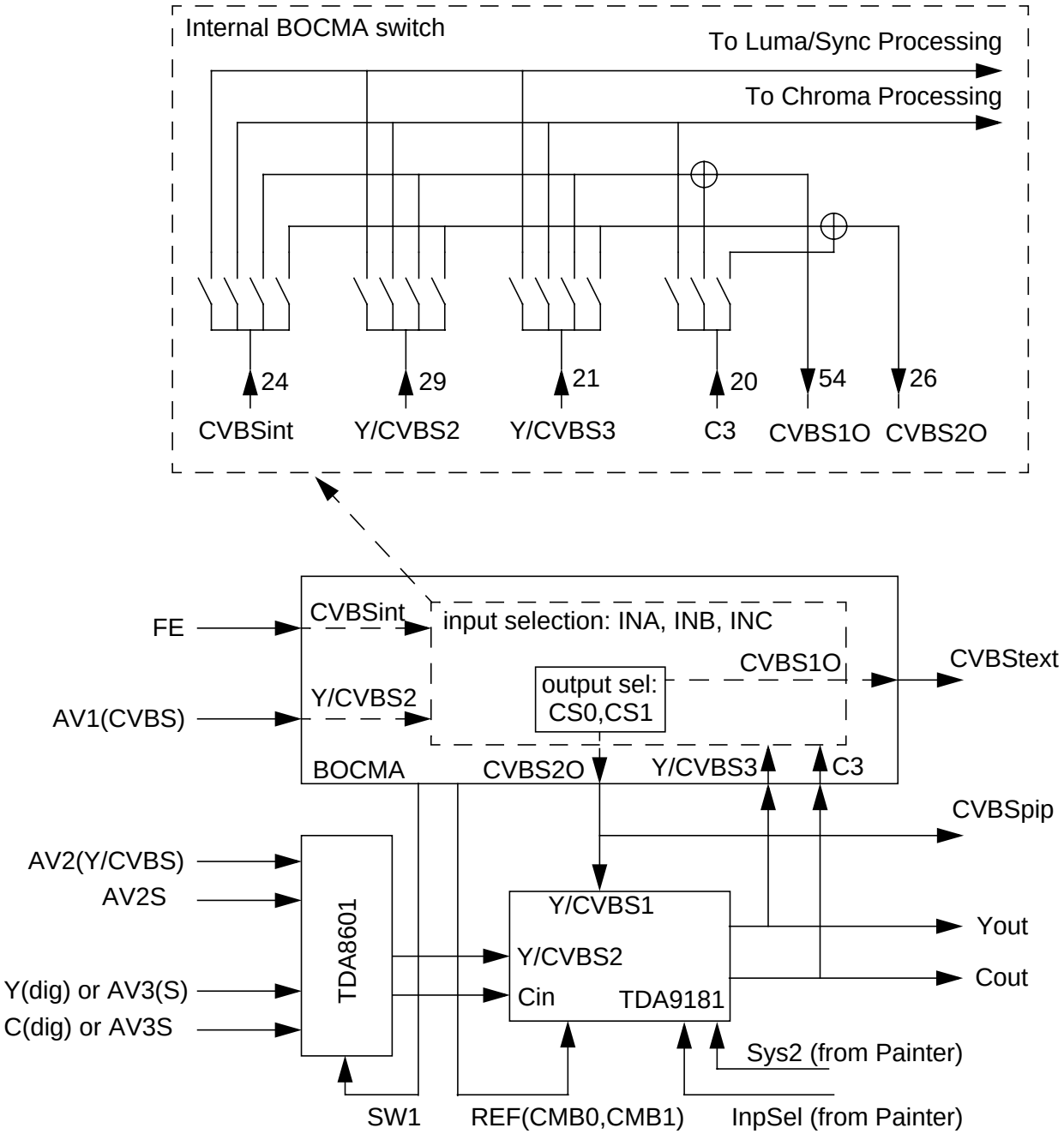



Fig.11 Peri & switching block diagram

In the internal BOCMA switch CVBS1O is identical to the selected signal that is applied to the internal video processing, so coupled to the displayed source. This output can be used for teletext aquisition and is therefore routed to the Painter. CVBS1O can also be used to make a video monitor output which is needed for the Asian market.

CVBS2O can indepently be switched to any input with bits **CS0,CS1**. This output is used for PIP **or** a

comb filter. The PIP application in combination with a comb filter can be made with an extra source switching IC for PIP. The comb filter only application is implemented.

The next table shows all the bit and pin settings for the peri switching.

**TABLE 4 Peri switching bit & pin settings**

| Mode | INA | INB | INC | CS1 | CS0 | SW1 | CMB1 | CMB0 | InpSel |
|---|---|---|---|---|---|---|---|---|---|
| FE | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| FE+comb | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| AV1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| AV1+comb | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| AV2 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| AV2+comb | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| AV2S | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| AV3 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| AV3+comb | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| AV3S | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |

**INA,B,C**=1,1,1 bits selects the Y3/C3 BOCMA inputs, this is for all SVHS and comb filter modes.
**INA,B,C**=0,0,0 bits selects CVBSint (FE).
**INA,B,C**=0,0,1 bits selects Y/CVBS2 (AV1).
**INA,B,C**=0,1,1 bits selects Y/CVBS3 (AV2/AV3).
Bits **CS0,CS1** are always zero except for the AV1 mode. In this situation the Y/CVBS2 input of the BOCMA has to be switched to CVBS2O to be able to comb AV1.
Pin SW1 (controlled by BOCMA bit SW01) switches between AV2(S) and AV3(S). In all other cases it is a do not care, but defined as zero in the table.
Bits **CMB1** and **CMB0** sets comb filter on and off: 10=off, 01=on.
Pin InpSel (controlled by Painter) is the switch between FE/AV1 and AV2/AV3.

The BOCMA 64QFP (all TDA888XH versions) has apart from the RGB input for OSD, a second RGB input which is used for AV1 RGB mode. There is also the possibility to set this input to YUV mode via bits **YUV2, YUV1, YUV0**. Two versions of YUV input levels can be selected, the internal Philips one (Y=1.4V, U=-1.33V, V=-1.05V) or the YPbPr version (Y=1V, U=0.7V, V=0.7V) which is used by e.g. DVD players.
If the YUV interface in not used, it can be set as a third RGB or YUV input, e.g. to support two full SCARTS both having RGB input capability or implement one full scart in combination with an YUV DVD input.
In this receiver design the YUV interface is implemented, to this connector a YUV input board can be connected to evaluate a YPbPr input. The embedded software does not support such a configuration.

### 3.4.1 AV Status detection for SCART

Pin 8 of a SCART output device can be used by the receiving SCART input device to put itself in the correct status. The SCART standard for the status pin 8 (called slow switching function pin) is listed below.

**TABLE 5 SCART pin8 status voltages**

| Pin 8 voltage [V] | Status |
|---|---|
| 0<Pin8<2 | No signal present |
| 2<Pin8<4.5 | Detection gap |
| 4.5<Pin8<7 | Signal present; 16:9 |
| 7<Pin8<9.5 | Detection gap |
| 9.5<Pin8<12 | Signal present; 4:3 |

AV status detection is done via StatAv pin. The StatAv pin is made by means of a long tailed transistor pair, the two status inputs of the SCARTs are the inputs. This is the most cheap detection of two SCARTS. The disadvantages are that the priority is fixed in the hardware, Av1 overrules Av2 status and when AV1 is active AV2 can not be evaluated. StatAv output voltage controls the source selection and sets the proper picture size although it can overruled by the user menu's source select and zoom menu. The StatAv is read via an ADC input in the Painter which decodes the status according to the next table.

**TABLE 6 AV status detection**

| AV2 pin8 | AV1 pin 8 | StatAv | Status | Rounded values for the ADC programming |
|---|---|---|---|---|
| 4.5V | | 0.33V | AV2 16:9 | 0.2V |
| 7.0V | | 0.69V | | 0.8V |
| 9.5V | | 1.05V | AV2 4:3 | 0.8V |
| 12V | | 1.40V | | 1.4V |
| | 4.5V | 1.71V | AV1 16:9 | 1.4V |
| | 7V | 2.81V | | 2.8V |
| | 9.6V | 3.85V | AV1 4:3 | >2.8V |
| | 12V | 3.85V | | >2.8V |

Note that StatAv detection is not supported by the current software.

## 3.5 TV Control Part: SAA55XX/56XX (Painter)

The micro controller can be a SAA55XX (Painter1) or a SAA56XX (Painter2) device. They are members of the micro controller family based on the industry-standard 80C51 core but now designed for television receiver control. They are available from non-text, 16kbyte ROM and 256 byte RAM, to a10 page text version, 128 kbyte program ROM and 2.25 kbyte of RAM for Painter 1.
Painter 2 is available with ROM sizes from 128 kbyte and 192 kbyte, also up to 14 kbyte RAM.

The different functions with the associated control lines are described in next the sub-paragraphs.

### 3.5.1 Control lines to the digital reception part

Five control lines are defined, these line are: reset_ext, PIOa, PIOb, PIOc, PIOd. These control lines go to the digital board of the receiver. Reset_ext can reset the MIPS via the Painter. PIOa, PIOb, PIOc and PIOd are reserved for future options.

### 3.5.2 Control lines to the comb filter

InpSel, Sys2. These control lines are needed when a comb filter is used.
OutSel is not used in this comb filter application, but still routed to the Painter. It must be kept floating! Pull-up resistor R58 and series resistor R53 must be removed.

### 3.5.3 Local Keyboard

The local keyboard is connected via four wires to the chassis:

- +3.3V standby
- Ground
- Remote Control Line (Rc5N)
- One analogue keyscan input (ADC), mutilplexed with a LED output

Via a resistor network and switches a specific analogue voltage is generated when a key is pressed. The nature of this network automatically excludes double key presses (lowest value wins). Normally the keyboard scan pin is only scanned during a few micro seconds, e.g. 8 times per second. The rest of the time it functions as a LED driver output, e.g. for remote control acknowledge, stand-by or error signalling. The LED is continuously emitting low intensity light to indicate that the TV set is “ON” (via a leakage resistor). During stand-by the micro controller sets the keyboard line high. Via a transistor this illuminates the LED at high intensity. Because the key scan line is high during stand-by, it is possible to implement a local keyboard “wake-up” to get the micro controller out of IDLE or POWER-DOWN mode.

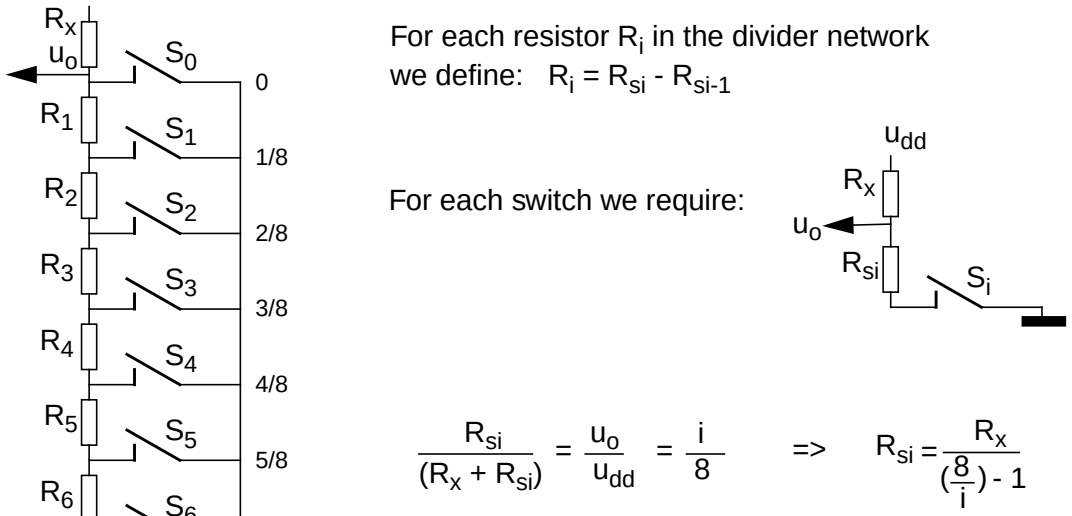



Fig.12 Analogue keyboard resistor network

TABLE 7 Calculation of local keyboard resistors

| Switch i | $R_{si}/R_x$ | $R_i/R_x$ | | @$R_x$=1k2 | Practical resistors | | Resulting value | Desired = i / 8 | (i/8+1/16) x $2^8$ 8-bit ADC window |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | | 0.0 | 0.0 | $00_H$ .. $0F_H$ |
| 1 | 1/7 | 1/7 | 0.143 | 171 | $R_1$ = | 180 | 0.130 | 0.125 | $10_H$ .. $2F_H$ |
| 2 | 1/3 | 4/21 | 0.190 | 228 | $R_2$ = | 220 | 0.250 | 0.250 | $30_H$ .. $4F_H$ |
| 3 | 3/5 | 4/15 | 0.267 | 320 | $R_3$ = | 330 | 0.378 | 0.375 | $50_H$ .. $6F_H$ |
| 4 | 1 | 2/5 | 0.4 | 480 | $R_4$ = | 470 | 0.5 | 0.5 | $70_H$ .. $8F_H$ |
| 5 | 5/3 | 2/3 | 0.667 | 800 | $R_5$ = | 820 | 0.627 | 0.625 | $90_H$ .. $AF_H$ |
| 6 | 3 | 4/3 | 1.333 | 1599 | $R_6$ = | 1k5 | 0.746 | 0.750 | $B0_H$ .. $CF_H$ |
| (7)[1] | (7) | (4) | (4) | (4800) | ($R_7$) | (4k7) | (0.873) | (0.875) | $D0_H$ .. $FF_H$ |
| none | - | - | - | - | | - | 1.0 | 1.0 | |

1. In practice the highest level of > 7/8 can not be used because of internal protection diodes.

Normally the keyboard is scanned about 8 times per second, during a few micro seconds. The rest of the time the keyboard line functions as an output, to drive a LED. The switching over from ADC-input to LED-output and back is not visible on the light output. The LED has the following functions:

- to flash an acknowledge, each time a valid remote control command is received
- to indicate that the receiver is powered, during stand-by (high lighted)
- to indicate that the receiver is on (low lighted), e.g. when the picture is dark
- to signal errors, detected by the software

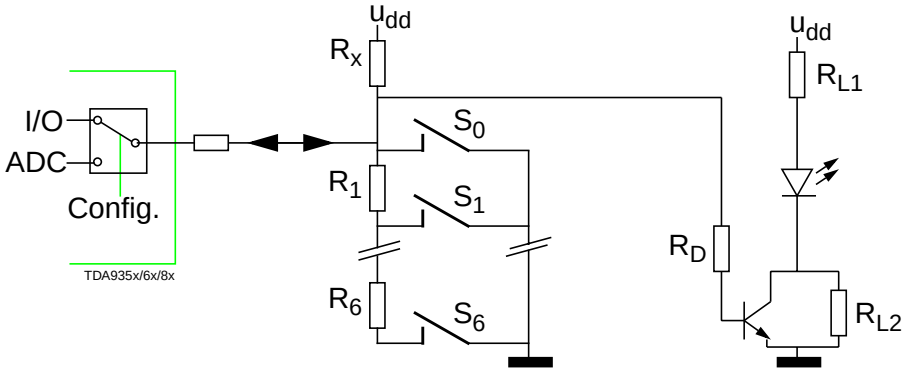



Fig.13 Multiplexed key scan and LED drive

Resistor $R_D$ is high ohmic enough (10 x $R_1$+..+$R_6$),to be not of influence on the keyboard ladder network. $R_{L2}$ is added to make the LED glow continuously (low lighted), as a Power-On signal.

### 3.5.4 CVBSText

CvbsText; Cvbs with teletext information in the VBI (Video Blanking Interval) lines which will be decoded by the Painter.

### 3.5.5 OSD RGB outputs

The RGB outputs from the Painter TV micro controller are current sources. Also the RGB DAC outputs from the SAA7215 AVGD are current sources. With a resistor to ground the RGB current is converted to a driving voltage for the BOCMA. Via the Fbl1 pin the internal BOCMA RGB-switch between RGBin and internal video is controlled. A voltage between 0.8V and 3V is detected as fast-blanking signal. In the hybrid receiver the RGB outputs from Painter and SAA7215 are via series resistors directly connected. In this way an adder is made and an RGB switch is not necessary as long as it is prevented that both devices do not produce overlapping OSD's at the same time, otherwise the OSD is mixed.

The BOCMA has a half-tone (HALFT or contrast reduction) input pin which can be driven by the CorNot output pin of the Painter. This Painter pin is coupled to the internal OSD generation and forced low inside OSD boxes. The BOCMA reduces the contrast of the underlaying video with 6dB while the OSD is displayed with normal contrast.

### 3.5.6 Synchronization of micro

OSD synchronization input signals Hsync and Vsync are derived from the deflection part to get a stable OSD picture on the television screen. The polarity of these signals is active high.

When real-flat picture tubes are used, the EW parabola correction has a much larger range than for conventional tubes. Now Hsync can not be coupled to the Hflyback pulses since they are modulated by the EW parabola during vertical scan. The result would be distorted OSD. This is also the case for conventional tubes with less EW modulation but than it is less visible. The OSD Hsync has to be coupled directly to the video sync. This is done by using the burst key pulse which is via the Phi-1 loop coupled to the incoming video. The differential pair T13, T14 biased at 4V is used as comparator to produce a burst key related Hsync pulse.

### 3.5.7 Reset and supply-voltage-guard

This demo receiver has a sophisticated reset and supply voltage guard circuit, which triggers the micro controller reset and EEPROM power supply. Most micro-controllers have an internal power-supply guard which will generate an internal reset once the supply-voltage drops below a threshold level. During this reset the outputs do have a defined output condition (most of the time floating). However when the supply falls further, even the internal circuits of the micro stops functioning. This may lead to unpredictable bouncing of the outputs. Because the $I^2C$-bus is controlled by such outputs, a burst of pulses can appear on the clock and data-lines. This can lead to un-wanted write actions, because some EEPROMs keep on functioning at very low supply voltages.

Once the supply-voltage starts to fall, an external reset is generated before the internal reset becomes active (even if the supply has a falling glitch the external reset will get a defined duration). At the same time the EEPROM supply voltage is switched-off

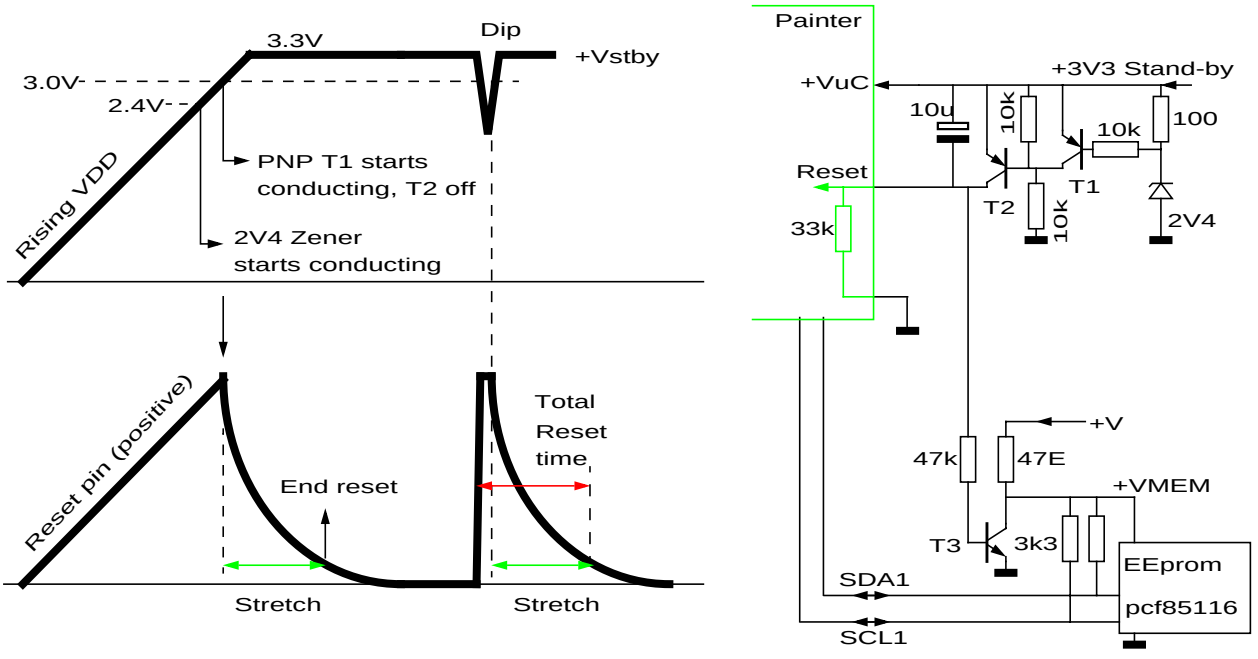



Fig.14 Reset and supply voltage guard circuit

The discrete reset circuit takes care that the (positive) reset remains active (high) as long as the 3.3V is below minimum operating level (< 3.0V). When the voltage has become high enough, the reset time is extended (charge time of reset capacitor) to guarantee a minimum safe reset time for the internal

micro controller. The supply voltage guard will immediately short circuit the reset capacitor when the 3.3V dips below < 3.0V. This fast-attack and slow-decay assures a proper reset, even on supply voltage spikes. At the end of the reset period (reset level < 0.5V), an NPN transistor T3 will enable the power supply to the EEPROM (and its $I^2C$-bus pull-ups). This assures that the EEPROM can only operate while the micro controller is running

The circuit description refers to the previous picture. Advantages of this circuit are the:

- well defined reset duration after reaching a well defined supply voltage.
- guaranteed reset pulse even after a short supply voltage dip.
- power control of the EEPROM.

## 3.6 Digital TV Sound Part: TDA9875A (DTVSP)

The small signal board also contains a full multistandard TV sound demodulator, decoder and processor for all stereo 2CS (A2, A2+) and Nicam (Nicam-B/G, I, D/K, L) and mono standards (4.5, 5.5, 6.0, 6.5MHz). This device supports three stereo inputs and one mono input. The mono input is used for the AM demodulator output from the BOCMA.
Via an internal Digital Sound Processor several sound processing features are implemented, like volume control, bass/treble, balance (for main speaker channel and separate for headphone).
Via the expert mode of the DSP the Philips ‘Incredible Surround” feature can be activated. This algorithm gives a wide stereo image with conventional TV loudspeaker setup at the corners of the cabinet. The perception is that the loudspeakers seem to be positioned with 3 meters distance in between, like in a normal stereo speaker setup.

Since the TDA9875A is a full digital device, some output pins have series coils to reduce the radiation of the internal clock spurious (at SIF input, IIC pins and supply pins) or series impedances and filter capacitors to ground (on all audio in- and outputs). When not used, via IIC the SYSCLK output can be switched off.

## 3.7 Sound Options: (Virtual) Dolby Surround Pro Logic

The TDA9875A sound features can be expanded with an additional optional DSP interfaced via IIS ports. It can be implemented as a separate (piggy back) add-on board connected to the sound add-on connector P19 on the small signal board.

In this receiver design no sound add-on applications are worked out but several options are described here. They should be seen as examples. Two add-on DSP’s are available, a third DSP is almost available and a fourth option is to implement AC3 decoding (although this is maybe too expensive to combine it with this mid-range 50Hz concept). The sound add-on connector can support all these options.

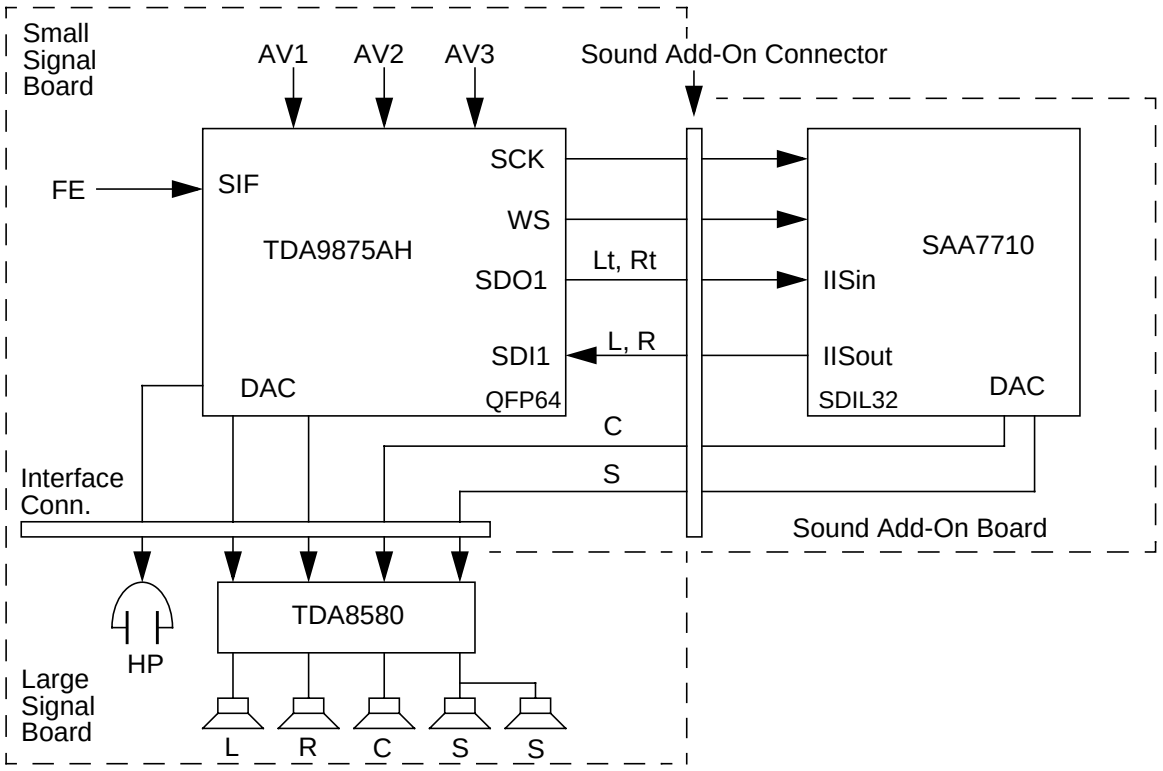
### 3.7.1 Dolby Surround Pro Logic with SAA7710

The SAA7710T chip is a high quality audio-performance digital add-on processor for digital sound systems. It provides all the necessary features for complete Dolby Pro Logic surround sound on chip. In addition to the Dolby Pro Logic surround function, this device also incorporates a 5-band parametric equalizer, a tone control section and a volume control. Instead of Dolby Pro Logic surround, the Hall/ matrix surround and Incredible sound functions can be used together with the equalizer or tone control.

SAA7710 features:

- Two stereo I2S-bus digital input channels
- Three stereo I2S-bus digital output channels
- I2C-bus mode control
- Up to 45 ms on-chip delay-line (fs = 44.1 kHz)
- Optional clock divider for crystal oscillator
- 4-channel active surround, 20 Hz to 20 kHz (maximum 1/2 fs )
- Adaptive matrix
- 7 kHz low-pass filters
- Modified Dolby B noise reduction
- Noise sequencer
- Variable output matrix
- Sub woofer
- Centre mode control: on/off, normal, phantom, wide
- Output volume control
- Automatic balance and master level control with DC-offset filter
- Hall/matrix surround sound functions
- Philips “Incredible Surround” functions
- 5-band parametric equalizer on main channels left, centre, right (fs = 32 kHz)
- Tone control (bass/treble) on all four output channels (fs = 44.1 kHz).
- SDIL32 packag

Fig.15 Dolby Surround Pro Logic with SAA7710




### 3.7.2 Virtual Dolby Surround Pro Logic with SAA7712

The SAA7712H provides digital signal processing power in TV systems and home theatre systems. A DSP core is equipped with digital inputs and outputs, a 5-band parametric equalizer accelerator, a digital co-processor interface and a delay line memory. This architecture accommodates on-chip standard sound processing, incredible surround, Dolby Pro Logic Surround and other surround sound processing algorithms. The architecture also supports co-processing, e.g. to add to the processing power of the internal DSP core or for multi-channel surround decoding. All settings and parameters are controlled by an IIC-bus interface. The available interfaces support a high application flexibility. The DSP core communicates over 32 dedicated registers. The selected digital input is master for the data rate of the DSP core. This input can be selected among 2 slave IIS-bus inputs. The 4 outputs from the core are passed through 4 DACs and then routed to 4 output pins. Two master IIS-bus outputs and two master IIS-bus inputs can serve as an IIS-bus co-processor interface. Eight of the remaining registers are used for communication with the hardware equalizer, and eight for communication with the delay line memory. All IIS-bus inputs and outputs support the Philips IIS-bus format as well as 16, 18 and 20-bit LSB-justified formats.

SAA7712 features:

- 18 bits data width, 12 bits coefficient width
- 1 kbyte delay line memory suited for Dolby Pro Logic Surround.
- Inputs: 2 slave 18-bit digital stereo inputs: IIS-bus and LSB-justified serial formats
- 2 master 18-bit digital stereo inputs: IIS-bus and LSB-justified serial formats.

- Outputs: 4 DACs with 4-times oversampling and noise shaping, fed to 4 output pins and configurable from the DSP program, as left, right, front and surround channels of a Dolby Prologic
- 4-channel 5-band or 2-channel 10-band IIC-bus controlled parametric equalizer
- Dolby Pro Logic Surround/Dolby 3 stereo: noise generation: A pink noise generator is included for installation of the Dolby Pro Logic/Dolby 3 stereo mode
- Hall/Matrix Surround: when no Dolby Pro Logic Surround source material is available then this mode can be used to produce a signal in the surround channel
- Incredible Surround (222-IS): This algorithm expands the stereo width (stereo expander). This is intended to be used when the 2 speakers are placed close together (TV set and Midi set).
- Robust Incredible Surround (222-RIS): Same as incredible surround only an alternative algorithm
- 3D Surround (422) or Incredible Virtual Surround: Dolby Pro Logic Surround reproduced by 2 speakers (L and R)
- IS-3D Surround (422-IS): Same as 3D Surround (422) only with extra stereo width expander on left and right
- RIS-3D Surround (422-RIS): Same as IS-3D Surround (422) with alternative algorithm
- 3D Surround (423) or Incredible Virtual Surround: Dolby Pro Logic Surround reproduced by 3 speakers (L, C and R)
- IS-3D Surround (423-IS): Same as 3D Surround (423) only with extra stereo width expander on left and right
- RIS-3D Surround (423-RIS): Same as IS-3D Surround (423-IS) with alternative algorithm
- Dolby B: both a Dolby B encoder and a Dolby B decoder are implemented
- 2 Room solution: In all modes not requiring more than 2 output channels (stereo and karaoke incredible surround) it is also possible to feed the source signal to the other 2 output channels (with same processed or not processed signal)
- Dynamic Bass Enhancement (DBE): Dynamic bass enhancement generates a sub-woofer channel, which is either a separate output or is added to the front channels
- Volume processing: Independent volume processing of all 4 output channels
- AC-3/MPEG-2: Inputs available intended to be used with an AC-3/MPEG-2 co-processor. In this mode the SAA7712H can be used as post-processor.
- Output redirection: Several output configurations are possible (normal 4 channel, special 4 + 2 channel, record 2 + 2 channel, 6 or 6 + 2 channel).
- Depending on the sample frequency, several combinations of the above mentioned features are possible.
- QFP80 package

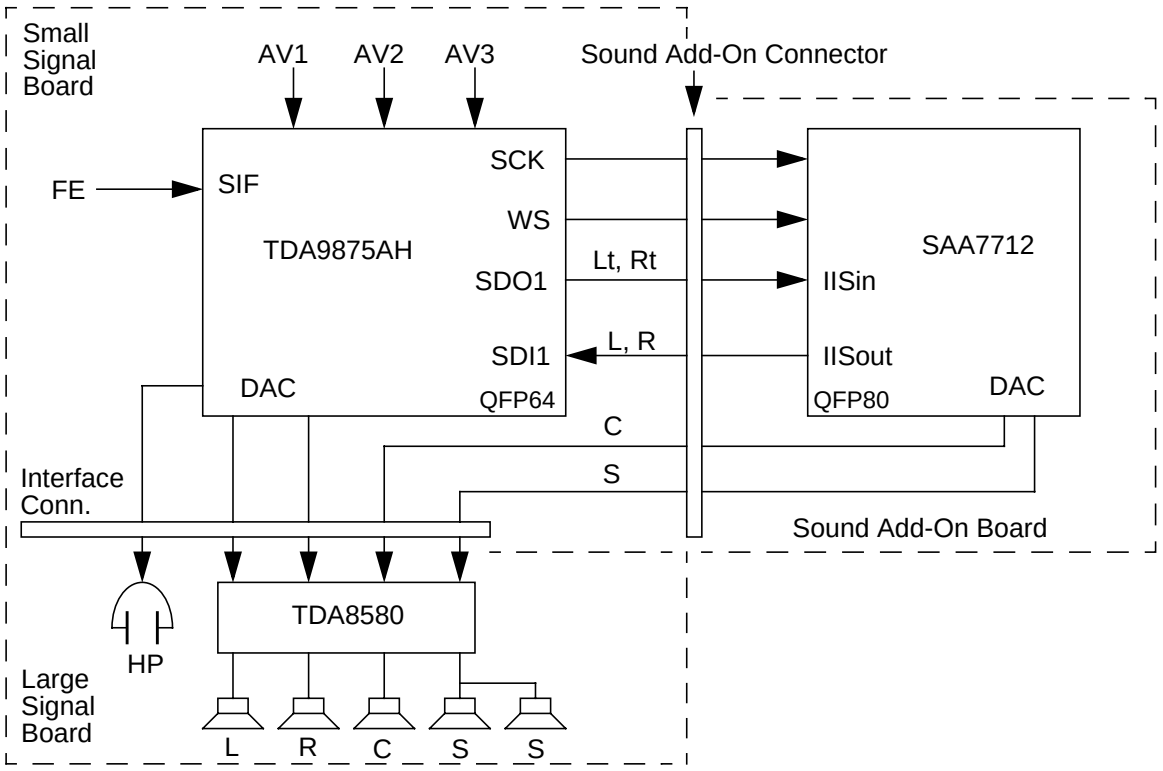



Fig.16 Virtual Dolby Surround Pro Logic with SAA7712

### 3.7.3 (Virtual) Dolby Surround Pro Logic with new SAA7715

The new design architecture makes the SAA7715 a very flexible programmable DSP that can be used in many applications. The device has three digital data inputs and can be driven in synchronous or asynchronous mode. In asynchronous mode the master source selection determines the output sample frequency while the other inputs, which may have other sample frequencies, are sample rate converted.

- 2K words (32 bits) DSP RAM
- approx. 65 MIPS processing power
- 8 - 20MHz clock input range
- Four IIS digital inputs related to one master WS & BCK input
- Three IIS digital outputs
- One stereo analogue output
- Sample rate frequencies: 32kHz, 44.1kHz, 48kHz and 96kHz
- 256Fs in/output mode
- Dolby (Virtual) Surround Pro Logic decoding with additional audio features
- Post processor for AC3/MPEG2 systems

- QFP44 package

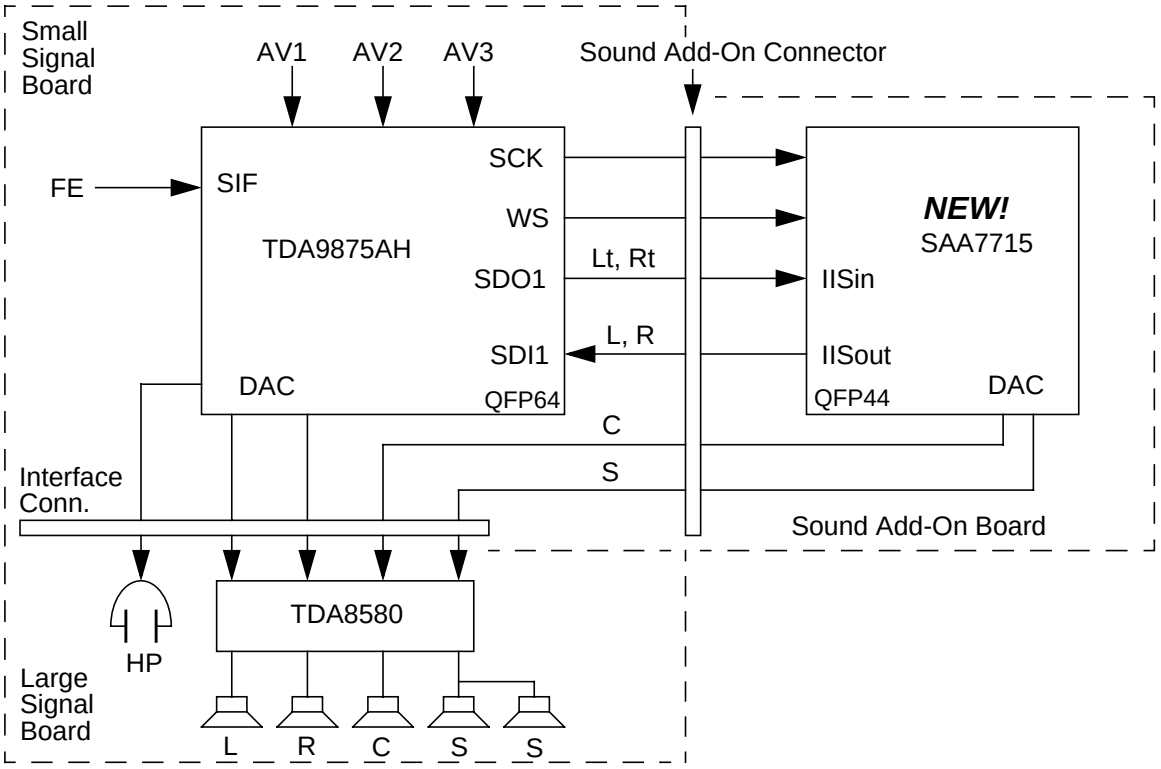



Fig.17 (Virtual) Dolby Surround Pro Logic with new SAA7715

### 3.7.4 AC3 decoding with SAA2505 and post-processing with SAA7715

The SAA2505H decodes multi-channel audio up to MPEG 7.1, AC-3 5.1 and pro-logic on a dual DSP core. The device contains all of the RAM and ROM necessary for operation. This minimises the need for external components and no micro code download is required. The device is primarily intended for audio/video surround sound applications. The input interface is made for SPDIF (IEC 60958) and formatted for the I2S-bus. The primary device output is PCM, sent via four I2S-bus ports. There is also a SPDIF (IEC 60958) formatted output. User control is achieved via an I2C-bus. However, the SAA2505H is capable of stand-alone operation.

SAA2505 features:

- Two 40 MIPS 20-bit DSP cores
- All input and output buffer RAM is on-chip
- Program ROM on-chip for all decoding modes
- Two I2S-bus inputs with normal, double and quad speed mode (slave only)
- Second serial input usable for ADC (Karaoke input)
- Three normal and double speed I2S-bus outputs (slave and master of 256 and 384fs )
- One normal, double, quad speed I2S-bus output (slave and master of 256 and 384fs)
- Japanese EIAJ serial input and output formats

- Sony Philips Digital Interface (SPDIF) output
- I2C-bus control (up to 400 kHz)
- MPEG 2 L2 up to 7.1 channels
- MPEG 1 L2 (Video-CD) 2 channels at 44.1 kHz
- Dolby pro-logic decoding at 32, 44.1 and 48 kHz
- Output configuration for 7, 5, 4, 3, 2 and 1 channels with or without Low Frequency Enhancement
- Bass redirection for small satellite loudspeakers plus subwoofer
- Karaoke voice mix
- Dynamic range compression (AC-3 and MPEG)
- Adjustable delay up to 15 ms for surround channels (1.5 kbyte words)
- Adjustable delay up to 5 ms for centre channel (250 words)
- QFP64 package

# 4. Digital Reception Part

## 4.1 Introduction

This chapter describes the digital part of the hybrid demonstration receiver which was demonstrated at the IFA'99 exhibition at Berlin. This digital part converts a digital Low-IF signal or an external transport stream to analogue Y/C and left/right analogue sound.

First a block diagram is introduced, then the digital demodulator and its application is described. The MPEG-2 source decoding and its memory configuration are given in the following paragraphs. At the end of the chapter the board interfaces and some debug issues are described.

## 4.2 Block Diagram Digital Part

The digital part of the receiver converts the QAM modulated DVB-C Low-DIF (Digital IF) carrier via an MPEG-2 source decoding part with an integrated DENC (Digital ENCoder) to analogue video in Y/C format and analogue left/right sound. Analogue Y/C video goes to the TDA8885 (one chip video processor) where video is further processed and displayed on the picture tube. THe Y/C format is chosen to have all the picture improvements of the TDA8885 available for the digital video. Analogue sound is directed to a TDA9875AH sound processor. Since TDA9875A has no options for sample rate conversion (DVB can have 32, 44.4 and 48 and maybe 96kHz sample rate), the TDA9875A sample rate is fixed at 32kHz (as needed for NICAM). As an additional sample rate convertor is too expensive, DVB audio is converted to analogue signals.
The OSD/Graphics generated by the SAA7215 are converted to analogue RGB signals and connected to the TDA8885 OSD RGB inputs. In the preparation phase of this hybrid reference design, the DVB-C QAM demodulator TDA8048 was on the IC roadmap. This product will now be replaced by the

VES1820 and derivatives of it. For more information of TDA8048 see ref. [1]. The application of the VES1820 or successors for this reference design is not implemented yet.

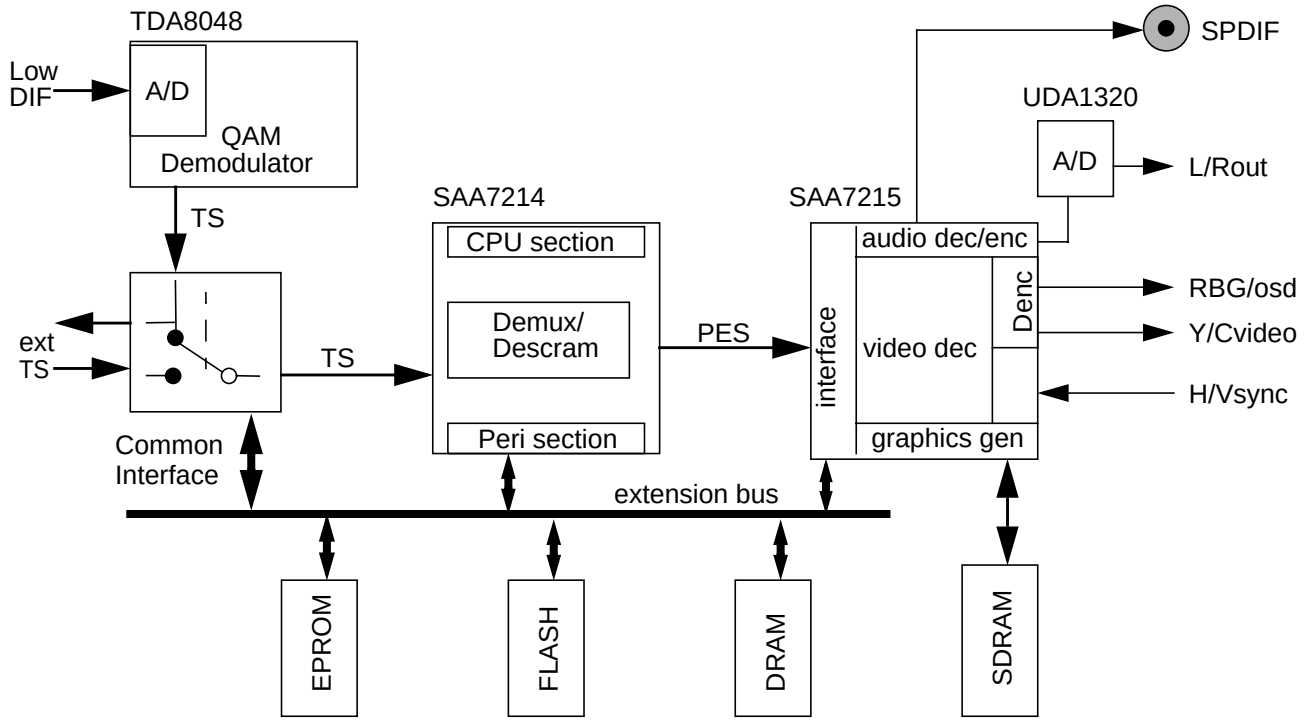



Fig.18 Block Diagram Digital Part

DIF, received from the analogue part of the LMR-DTV, is demodulated to a TS and goes to a common interface chip. There is also the possibility created to insert a TS from an external source, so no front end is needed. After that the TS is demultiplexed in the SAA7214 (MIPS). This MIPS has an extension bus where memories, common Interface and the SAA7215 is hooked on. The output from the MIPS goes to the SAA7215 (AVDG decoder) which decodes audio and video and generates OSD/graphics. This decoding is done in the SDRAM. The decoded digital audio is converted into analogue with the help of the UDA1320, also a connector is made for digital audio out (SPDIF). Analogue video (Y/C signal) goes to the TDA8885, picture improvement can be done there. OSD/Graphics is inserted in the BOCMA via the RBG out of the SAA7215. H/Vsync in are needed when video from the TDA8885 and OSD/Graphics from the SAA7215 is required.

## 4.3 DVB channel decoding

### 4.3.1 DVB-C

The basic operation of the digital front end part is given below.

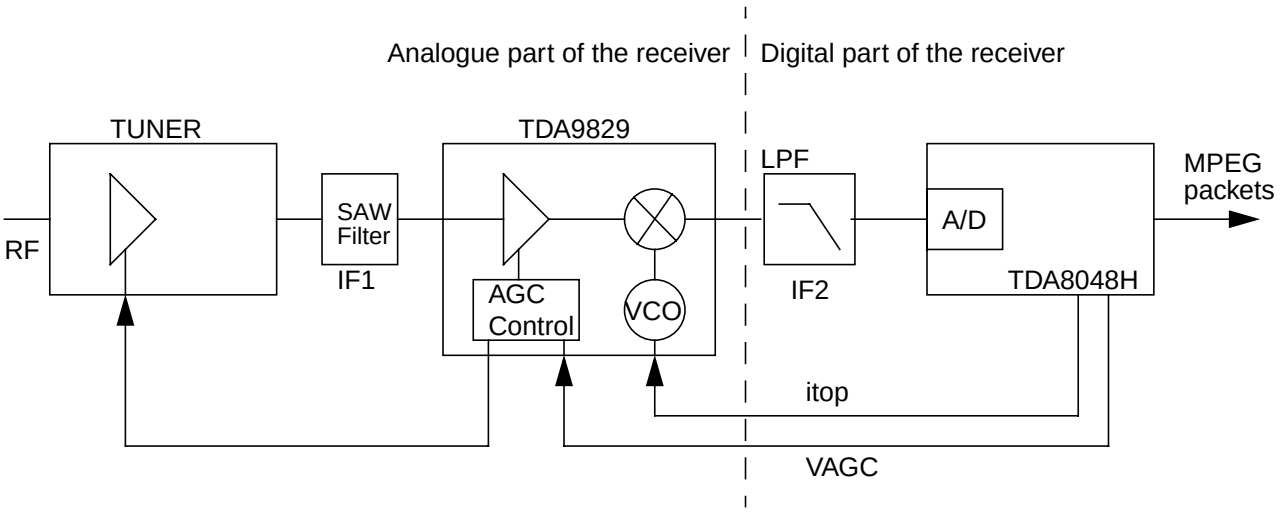



Fig.19 Block diagram digital front end

Digital front end is divided over the analogue PCB and digital PCB. This is because one tuner is required and it is not desired to use long tracks with IF signals on it.

RF signals are fed into the tuner, after which the TDA9829 performs DVB-IF processing. There IF1 (36.15 Mhz) is down converted to the symbol frequency IF2 (6.9Mhz)

For DVB-C IF processing of the TDA9829, the IF1 signal is first amplified to a level suitable for driving the ADC. The signal is mixed down to a lower frequency called IF2. The low pass filter is used to suppress remaining mixing products

After the LPF stage, the next stage is the internal AD-converter. After the ADC the next stage is the Cable Demodulator and the RS-Decoder (CDD).

The amplifier in the TDA9829 is gain controlled externally by the TDA8048. The TDA9829 also provides an AGC signal to the tuner. The AGC control characteristics of the internal amplifier and the tuner AGC are set by a Take Over Point (itop) circuitry. This AGC control approach results in a better noise behaviour and a larger AGC range.

The MPEG packets or Transport stream (TS) consists of: data[0..7], PKT_Strobe, PKT_Valid and PKT_Sync and goes to a Common Interface IC. This IC creates the possibility that e.g. a scrambled TS goes to an external decoder and that the decoded TS goes to the MIPS. This Common Interface is described later in the application note.

### 4.3.2 Application

This sub paragraph will handle some applications related to the TDA8048

To support advanced board testing facilities, a boundary scan test hardware, according to the JTAG standard is included. Solder paths are defined at the board.

#### 4.3.2.1 Low-IF ADC pre-filter

The main function of the low pass filter is removing the unwanted mixing products generated by the TDA9829 mixer. The nearest unwanted frequency components in the output spectrum are the oscillator frequency and the sum component at twice IF. The LPF is designed to suppress these components to 40 dB under the wanted component. The measured characteristic of the LPF is shown below.

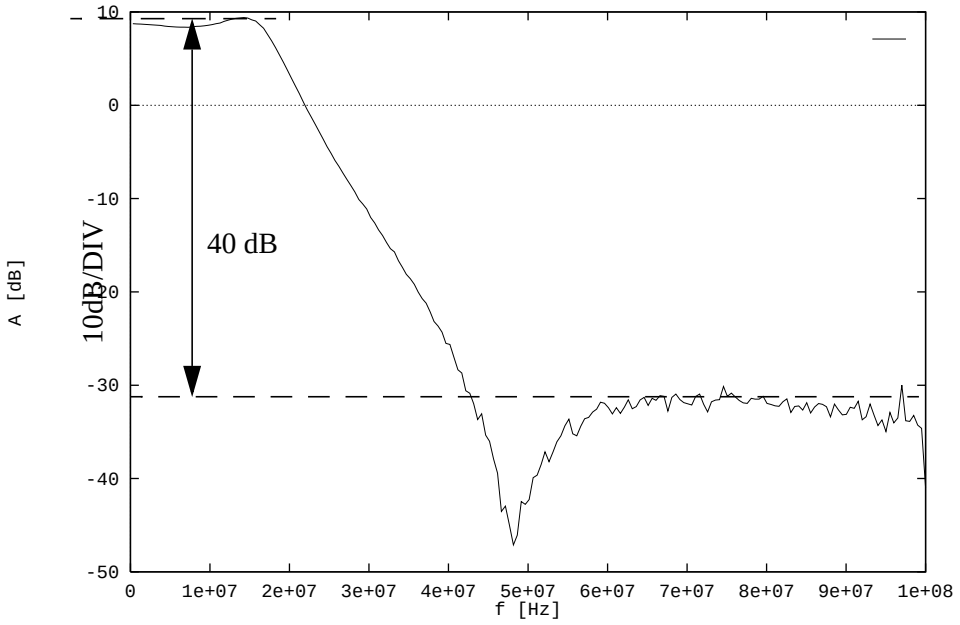



Fig.20 ADC pre-filter characteristic

#### 4.3.2.2 Input circuitry

The signal from the LPF filter is de-coupled by a capacitor and put on a DC level value of 2.5V by means of two resistors. The three analogue reference voltages (VRB, VRM and VRT) should be very clean, this is done via RC filtering.

#### 4.3.2.3 Crystal oscillator

The TDA8048H contains a build in crystal oscillator, requiring only a few external components; see figure below.

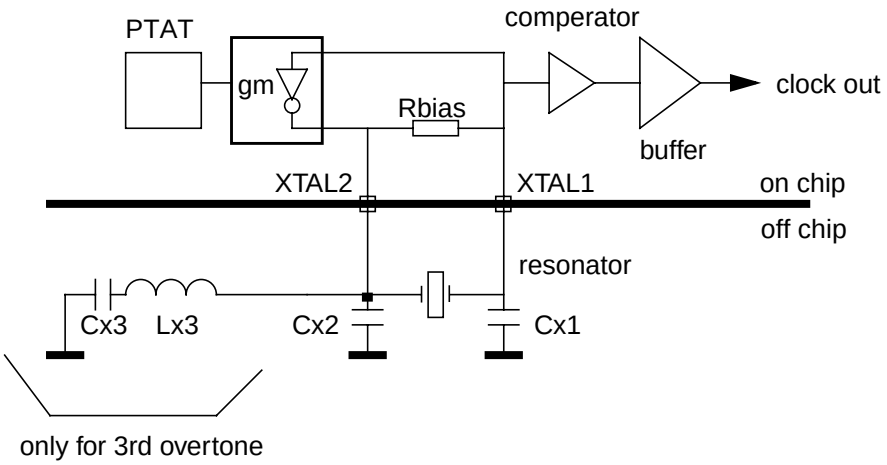



Fig.21 Application diagram of the crystal oscillator

The type of crystal used determines the use of the extra 3rd overtone components Cx3 and Lx3.

**TABLE 8**

| F range [MHz] | Cx1 [pF] | Cx2 [pF] | Cx3 [pF] | Lx3 [μH] |
|---|---|---|---|---|
| **Fundamental** | | | | |
| 20-27 | 15 | 22 | N.C. | N.C. |
| 27-35 | 10 | 18 | N.C. | N.C. |
| **3rd overtone** | | | | |
| 20-27 | 15 | 22 | 10 | 3.9 |
| 27-35 | 10 | 18 | 10 | 2.7 |

The equivalent model of the resonator is given below

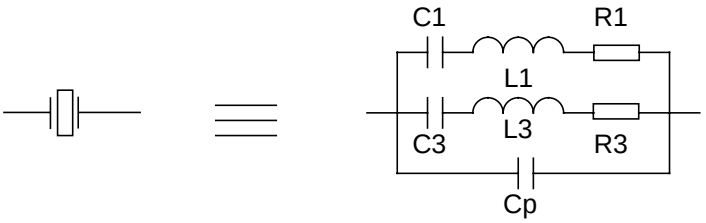



Fig.22 Resonator equivalent model

(C1, L1, R1) and (C3, L3, R3) are for the fundamental and third overtone oscillation modes while Cp is the package parasitic capacitance. For oscillation the requirements for the crystal are:
Cp < 7 Pf
R1, R3 < 100 Ω

#### 4.3.2.4 Preset

The Preset is active high; if generated it should be high for at least 5 clock periods of the Xtal. In the application the Preset is generated by the hardware during start up.

This is done be means of an RC circuitry. Important is that the RC delay of the circuit is not too slow compared with the set up time of the +5v supply. If so, the Preset value is too low and no reset is done. In that case the value of C or R should be increased.
Another possibility is to connect the Preset pin to the RESETn pin of the micro controller, this is not implemented in this concept.

#### 4.3.2.5 VAGC

The TDA8048H has two methods for AGC control, namely VAGC and IAGC. Chosen is for VAGC, this has the advantage that only an external RC network is required.

The VAGC output of the TDA8048H is an open-drain output. This output is pulled-up via a resistor to the supply voltage; a low pass filter converts the output (pulse train) to a control voltage.

#### 4.3.2.6 itop

ITOP is a current source and can be set via two IIC registers. One register sets the maximum current and the other controls the current. The adjustment input of the TDA9829 is designed to be controlled by a voltage. So a current to voltage conversion is made via a resistor. This conversion is done at the analogue board.

#### 4.3.2.7 Transport stream

The TDA8048H has a serial or a parallel output stream. The serial one is only for test purpose and is not used in the application. The parallel output has an 8 bit wide data stream and has four control signals. One, PKT_Bit_VALID, is not used. The used control signals are:

- PKTSYNC, a packet sync signal which is high during the first byte of a transport packet.
- PKTVALID, a valid output data signal indicating the difference between data and parity bytes.
- PKTSTROBE is a clock signal. At the rising edge TS(0:7), PKTSYNC, PKTVALID are valid.

### 4.3.3 DVB-T

When using a COFDM digital front end part, the TDA8048H is replaced by the VES9600.

## 4.4 MPEG-2 Source Decoder

The SAA7214, Transport MPEG2 source decoder, is able to receive and decode MPEG-2 transport streams, including de-scrambling, demultiplexing. In addition, it includes a PR3001 core which is a 32-bit MIPS RISC based CPU core and it has several interfaces.

Of the SAA7214 the following external interfaces are used:

- an extension bus supporting DRAM, EPROM, Flash, and a Common Interface.
  It also supports a synchronous interface to communicate with the integrated MPEG AVGD decoder SAA7215 at 40.5 MHz.
  For debug facilities also two DIN connectors are placed.

- One UART for debug mode.
- One UART is used to communicate with a micro controller, option not used
- Two IIC master/slave transceivers with DMA capabilities, supporting the standard (100 kbit/s) and fast (400 kbit/s IIC bus modes.
- 11 general purpose, bidirectional I/O interface pins; 4 of them are used as interrupt inputs. Two are reserved for future options, regarding to define the data bus size. One for the EEPROM and 4 are reserved for future options
- One PWM output (8 bit resolution), for controlling the 13.5 MHz system clock.
- A JTAG interface for board test support.

These interfaces will be explained in the following sub paragraphs

### 4.4.1 Bus structure

The extension bus handles all traffic between the SAA7214 and external memories, common interface and SAA7215. This is done by means of a 16 bits wide data bus, a 20 bits address bus and some control lines for the external memories, common interface and the AVGD decoder. The video SDRAM connected to the SAA7215 can be accessed from the SAA7214 through the extension bus via the SAA7215 interface. This way of direct accessing is not used at the current implementation.

### 4.4.2 Interfaces

UART(2); is defined to communicate with a micro controller. This option is not used in the receiver.

IIC bus of the MIPS (IIC1) is connected to the Painter on the analogue part of the receiver. This is done by means of solder jumpers, this possibility is made to connect this IIC bus to the main IIC bus of the analogue part of the receiver. The other IIC bus (IIC0) is connected with an EEPROM, TDA8048H and the CI.

In the EEPROM the user settings of the digital board are stored inside that memory. IIC address selection of the EEPROM is done via pin 1 (A0) and 2 (A1). In the hardware A1 is Vcc and A0 is GND, IIC address is A4Hex. Write protection is done at pin 7; when pin 7 is low, then write enable. A service pin at the MIPS is defined.

### 4.4.3 I/O Interfaces

The following i/o lines are defined.

pio[0], IRQ(CI); interrupt request from CI
pio[1], IRQ(8048); from TDA8048 cable front end demodulator
pio[2], IRQ(0); from SAA7215
pio[3], IRQ[1]; also from SAA7215
pio[4], pio[a]; reserved for painter; at the moment nc to painter
pio[5], pio[b]; also
pio[6], pio[c]; also
pio[7], pio[d]; also
pio[8] and pio[9] are connected via a 10K resistor to GND or via 10K to Vcc. So one has the possibility to start up in an 8, 16 or 32 wide data bus. This i/o control is not used in the SAA7214; this option is

prepared for the SAA7219.
pio[10], Service; this makes it possible to write the EEPROM.

### 4.4.4 Application

This sub paragraph will handle some applications related to the SAA7214.

#### 4.4.4.1 RESETn

This pin is an interrupt line. It is generated during start up, by means of an RC delay. Furthermore it can be made by the MIPS itself, e.g. sleep mode, error. Also the analogue part, by means of the Painter, is capable of giving a reset pulse. The reset can also act as a control output for the CI and flash memories. This pin is capable of delivering 8 mA output current.

#### 4.4.4.2 Oscillator/PWM[0]

According to the MPEG-2 system, information for clock recovery and synchronization of a selected program is regularly transmitted in the adaptation fields of MPEG-2 transport packets. This information is used to control the 13.5 MHz system clock of the SAA7214. Control is done via a PWM DAC of the SAA7214. This is needed because the frequency difference between the LMR-DTV local 13.5 MHz clock and the transmitter clock differs, so the variation of the VCXO is 13.5 MHz +/- 30 ppm. In the application the VCXO is made with discrete components. A simplified schematic is given below.

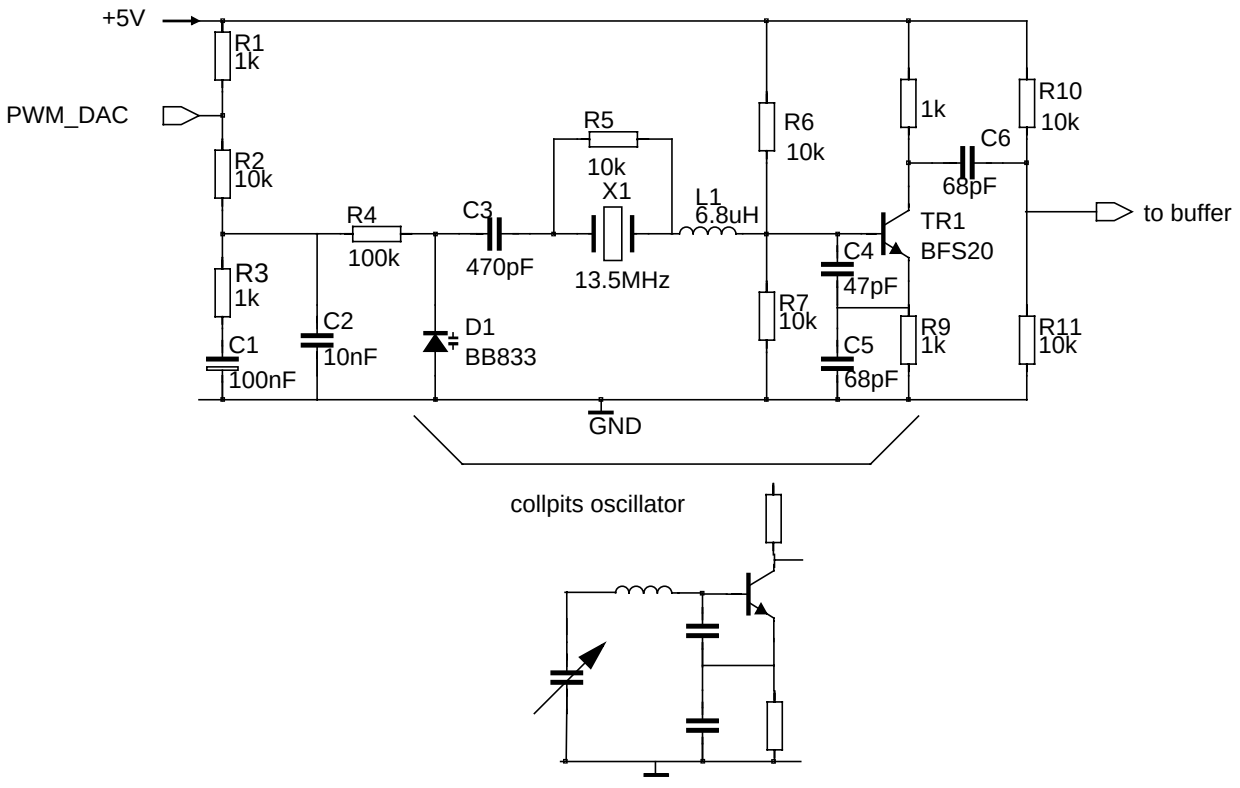



Fig.23 Oscillator circuitry

The signal from the PWM_DAC has a variable duty cycle, this depends of the DAC setting, this signal is made DC by means of R2 and C2 (filter R3 and C1 slows down control speed of the VCXO). When changing the duty cycle of the PWM_DAC, the DC voltage the varicap is changing. So the capacity of this varicap is also changing ($V_{reverse}$ is increasing then capacity is getting smaller). By this means the oscillator frequency can be changed. R5 and L1 are implemented to create more spread. The used oscillator is a collpits configuration (see simplified figure). The output of the oscillator is put at the collector side of the transistor, so the buffer has no influence at the emitter side of the oscillator.

## 4.5 AVGD Decoder

The SAA7215 is an Intergrated MPEG AVGD decoder which combines audio and video decoding. Additionally to these basic MPEG functions it also provides means for enhanced graphics, background display and/or OSD as well as encoding of output video.

### 4.5.1 Bus structure

The SAA7215 communicates with the SAA7214 by means of a bus structure. The bus has a 16 bit data bus size, 20 bit address bus size and six control and related signals. These signals are: siz[1], siz[0], DS (OEn), DTACKn, CS_RDn and CS_RGn.

### 4.5.2 Packet elementry stream

The decoder receives from the MIPS an 8 bit MPEG2 stream with three control signals, viz. A_STROBE, V_STROBE and AV_ERROR. A_ (Audio) and V_STROBE (video), high to low transition strobes the data in the AV_DATA stream. The AV_ERROR indicates the flag for a bit stream error.

### 4.5.3 SDRAM interfacing

The SDRAM is a high-speed CMOS synchronous DRAM containing 16 Mbit. Its interface speed is 81 MHz, data bus is 16 bit wide, address bus is 12 bit and 4 (SDRAM1)or 5 (SDRAM2) control lines.

The purposes of the SDRAMs are: MPEG audio and video decoding (SDRAM1); graphics data storage and scratch memory is done in SDRAM2. The external SDRAMs have self test capability, this is done by means of the software. The block diagram is given below.

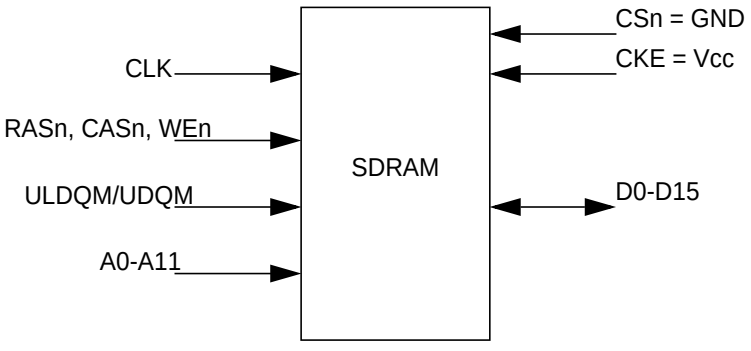



Fig.24 Block diagram SDRAM

#### 4.5.3.1 Application

The following pins of the SAA7215 are connected together:

- CP81M and CP81MEXT
- READ_OUT1 and READ_IN1
- READ_OUT2 and READ_IN2

### 4.5.4 Outputs of the SAA7215

The outputs of the AVGD decoder are in video and sound. Analogue video from the digital tuner goes to the TDA8885 via an Y/C signal. OSD/Graphics go via RGB outputs to the TDA8885. Sound is made analogue at the digital board before it enters the TDA9875AH.

#### 4.5.4.1 Analogue Video

To lock the deflection to the analogue video signals from the SAA7215, Y and C go straight to the TDA8885. Y/C signal is chosen because the picture improvement features from the TDA8885 can still be used (make use of Y/C and one can still use peaking and coring).

The RGB outputs deliver the OSD/Graphics. Because fastblanking is not implemented at the SAA7215, a work around is used. The Fbl function is made by means of the Graph pin of the SAA7215, the only restriction is that only one boxed OSD is possible.

If OSD/graphics are only generated by the SAA7215 and one has an analogue TV signal, one has to slave the SAA7215. This is done by inserting Hsync and Vsync into the SAA7215. These synchronization signals should only go from the analogue to the digital part and not vice versa. This is done via emitter followers, so only sync signals go from TDA8885 to SAA7215 and not the other way.

#### 4.5.4.2 Sound

The TDA9875AH (Digital TV sound processor) is only capable of receiving IIS with a sample frequency of 32 KHz. The SAA7215 is capable of handling the audio sample frequencies of 16, 22.05, 24, 32, 44.1 and 48 KHz. The IIS is converted via the UDA1320 to analogue sound signals.
Via an LPF these signals go to the TDA9875A. The UDA1320 delivers an output of 1000mV (rms value) and the TDA9875AH expects a value of 500mV so the signals are divided by two.
For future options IIS is directed to the digital/analogue connector; FSCLK is also an output on the digital to analogue connector.

## 4.6 Memory Configuration

The memory configuration which is connected to the extension bus consists of an EPROM, flash memories and a DRAM.

The EPROM is needed when a software update is required in the field. This update is done via the RS-232 connector instead of the debug connector. So the EROM acts is an interface, the updated software is stored in the flash memory. This memory is an OTP memory in a PLCC package. Device selection is done via CS and it has OEn control. VPP (program supply) and Pn (program) pin are not used in the application.

The DRAM acts as a scratch memory; variables and data which can not be set into the memory of the SAA7214 is put in the DRAM.

In the flash memory the digital system software is stored. Each flash memory has a storage capacity of 2 Mbyte, so in the application the software with the size of 4 Mbyte can be stored in the flash memories. It is a 3V3-only flash memory. This memory is designed to be programmed in-system with 3V3 supply. Internally generated and regulated voltages are provided for the write or erase operations.

BYTE (pin 47) is connected to Vcc, so a 16 bit data bus is used. RESETn (pin12) is connected to system reset. RY/BY (pin 15) is not connected; this output pin can be used to detect program or erase operation, not used.

The block diagrams of the different memories are given below.

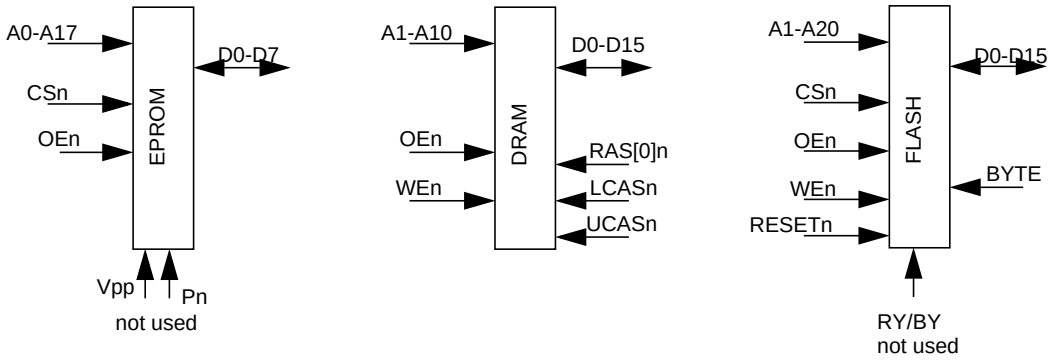



Fig.25 Block diagrams of the memories

## 4.7 Board Interfaces & Connectors

### 4.7.1 Common Interface

The common Interface is needed when e.g. a scrambled TS is used. This scrambled TS is directed to a connector and at the connector an intelligent device, e.g. smart card, is placed. There the scrambled TS is de-scrambled and via the connector the de-scrambled TS goes back to the CI. This connector is a PCMCIA connector. This is a 68 pins connector which is very familiar used in notebooks.

As an example the connector is hooked to the SAA7214 via a Dual CI hardware controller CIMaX$^{TM}$. This controller enables direct address to two independent CI modules. In the application only one CI module, module A, is implemented. It includes the necessary I/Os to interface the transport stream generated by the TDA8480H and to daisy chain it through a module and back to the SAA7214. Below a block diagram is given

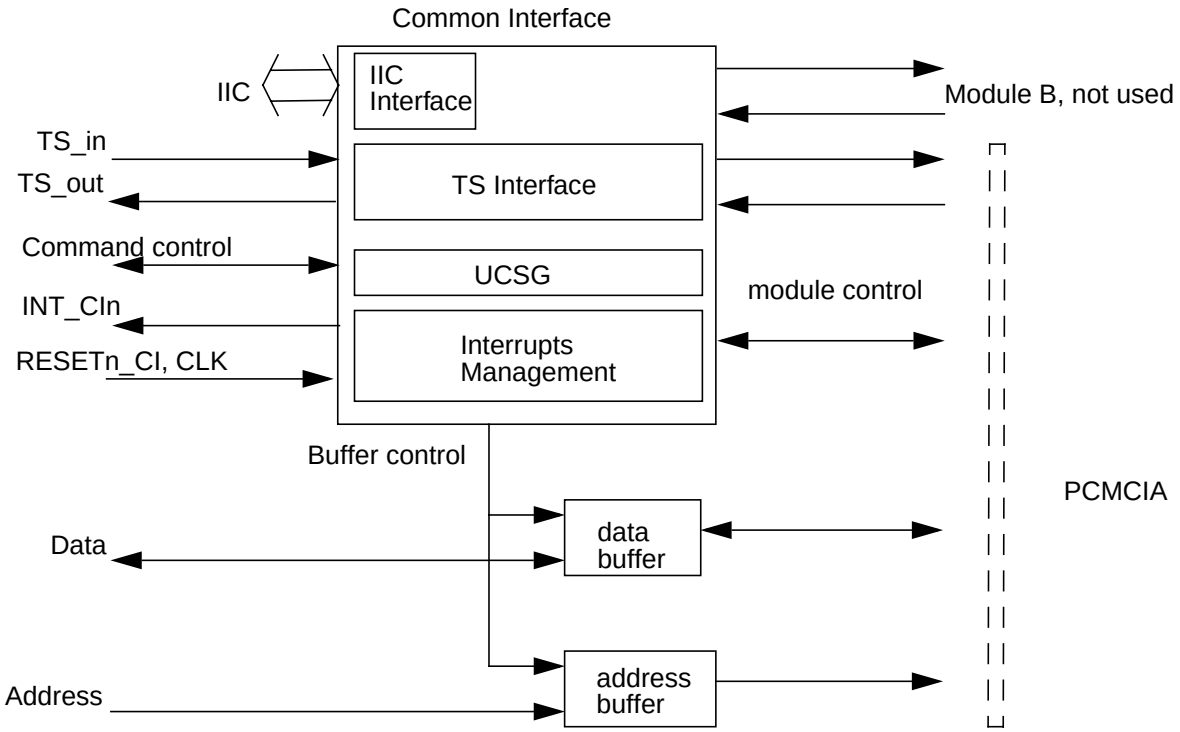



Fig.26 Block diagram of the Common Interface.

This CI has two logical interfaces. The Transport Stream Interface (MPEG-2) and the Command Interface (command control, data and address).The CIMaX$^{TM}$ interfaces with the SAA7214 by means of an IIC bus for initialization, while an Universal Control Signal generator (UCSG) maps a CPU control bus into the Command Interface control signals. The command interface control signals are: CS, WR, RD, INT and ACK.

To minimize pin count, the address and data bus from the SAA7214 transit through external buffers that are driven by the CI device. The 15 bits address bus has a 74LVT16373A buffer (16-bit transparent D-type latches). When ADOE# and ADLE are high, addressing is done via the PCMCIA connector. The buffer of the 8 bits data buffer is a 74LVT245 (octal bus transceiver). DATOE# is active-low (data transmission possible). When when DATDIR# is high then data from SAA7214 to connector; when DATDIR# is low then data from connector to SAA7214.

IIC addressing is done with pin 32 (SA0) and pin 33 (SA1) of the CI device. In the hardware Hex80 and Hex82 can be chosen by means of a solder jumper at pin 32.

RESETn_CI; because the reset pin from the CI-IC is active high, the RESETn from the system reset has to be inverted; this is done via a transistor.

The CLK signal is 27 MHz clock from SAA7215.

The PCMCIA connector is not placed on the PCB; the signals end on a 32 pins dual header, so by means of a flat cable these signals can go to a PCMCIA connector. In case one does not want to use the CI one can skip the chip and place the 0Ω resistors to connect the TS from directly to the MIPS. Also the possibility is made to insert a TS from an external source into the MIPS without using the common interface device; this also is done via 0Ω resistors.

### 4.7.2 RS232

To monitor the software of the MIPS a Multichannel RS-232 driver/receiver is needed. This IC makes it possible to communicate with a +/- 12 V environment of the RS-232 protocol. So one can connect a PC to the digital part of the receiver. By this means one can monitor the software running om the T-MIPS via UART(0).

### 4.7.3 SPDIF

Serial SPDIF (IEC958) audio output contains two channels of decoded MPEG (LPCM) audio data or still encoded burst formatted multichannel audio e.g. AC-3. A buffer is placed to protect the AVGD decoder and the transformer is needed for galvanic isolation.

## 4.8 Debug Hardware Support

### 4.8.1 Debug connectors

For debug mode two 3*32 pins DIN connectors are placed, the connectors are placed in such a way that removal does not take a lot of redesign.

### 4.8.2 Boot from flash1 or ROM

The digital part of the board supports both boot from Flash or ROM. The following settings are required for the desired boot.

**TABLE 9 Boot settings**

| Required setting | R1141 | J1105 | J1104 | j1103 |
|---|---|---|---|---|
| Boot from ROM | fitted | not fitted | fitted | fitted |
| Boot from Flash1 | not fitted | fitted | not fitted | not fitted |

The boot pin (pin 154) is used to start up in an 8 or 16 bit wide data bus. Pin is high then 16 bit wide, low 8 bit wide.The boot selection is done via CS[0]n. *not used in LMR-DTV*

### 4.8.3 Download to flash

The following jumpers should be set when copying the software from a debug tool to a Flash memory 1. Place jumpers J1103, J1104 and J1106

### 4.8.4 JTAG

To support advanced board testing facilities a boundary scan test hardware, according to the JTAG standard, is included. Solder paths are defined at the board.

## 5. Power Supply & Deflection

### 5.1 Power Supply

The Switch Mode Power Supply part is build with the GreenChip TEA1504 SMPS controller and an external MOSFET switch to drive the transformer. The circuit can supply 200W.

In a later version of this report the power supply part will be decribed in more detail. For this moment one can read application note AN98011 which describes the 200W TEA1504 application board.

### 5.2 Horizontal Deflection

The horizontal deflection has the following parts: horizontal drive circuit, horizontal switch, diode modulator, line output transformer (LOT) and East-west amplifier.

The horizontal drive pulses from the TDA8885 are amplified by the horizontal drive circuit to get sufficient base-drive current for the high voltage switching transistor T. So the horizontal drive output (Hdrive) is pulled up via a 1k8 resistor to +8V situated on the deflection part of the board, followed by a buffer to sink enough current to switch off/on the driver transistor.

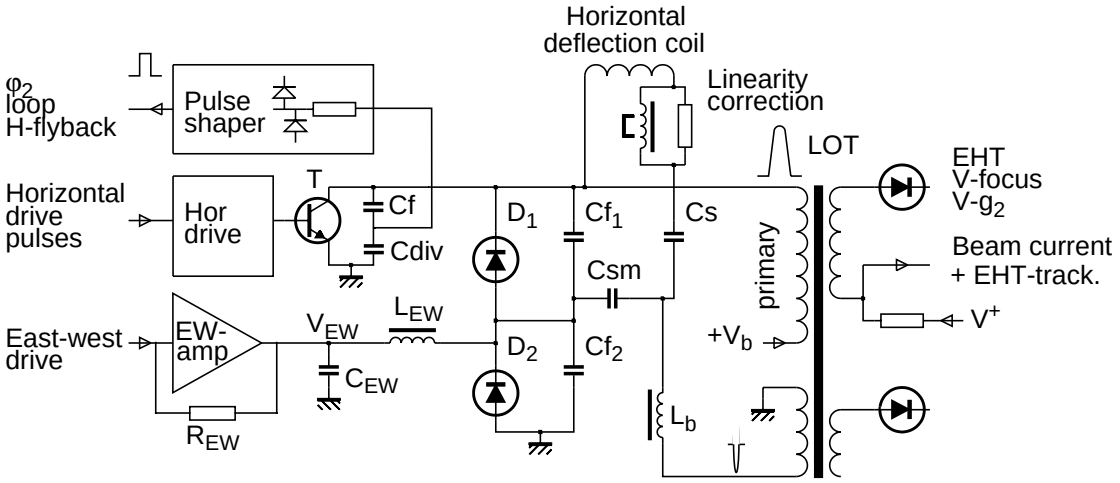



Fig.27 Functional diagram of the horizontal deflection

During the horizontal scan period (≈52µs) T and/or D1, D2 will conduct and an increasing (sawtooth) current flows from +Vb through the primary winding of the LOT (Line Output Transformer) to ground. At the end of the scan T, D1 and D2 are switched off. The energy stored in the LOT during the scan period, will now be transformed to the flyback capacitor Cf. This energy transfer will take place in a cosine shape because the primary of the LOT and Cf form a resonant circuit. The time the energy is transferred from LOT to $Cf_1$ and back to the LOT, is called the flyback time and will take place in about 12µS. The flyback peak voltage is about 8 times the scan voltage.

From this pulse we derive an H-flyback pulse to close the $\varphi_2$-loop. The pulse shaper can be e.g. a simple capacitive divider with two clipping diodes (from ground to H-flyback and from H-flyback to +8V). Note that the capacitor to ground is much larger than Cf so that it does not affect the resonance.

The diode modulator is modulating the horizontal deflection current without disturbing the amplitude of the flyback voltage on the primary of the LOT. Thus the EHT voltage remains constant and independent of the horizontal deflection current (picture width). The diode modulator is formed by $D_1$, $D_2$, $Cf_1$, $Cf_2$ and $L_b$ and the horizontal deflection coil. For a correct working of the diode modulator the resonance time of the following circuits must be equal:

- Cf with the primary inductance of the LOT
- $Cf_1$ with the horizontal deflection coil
- $Cf_2$ with $L_b$

The scan voltage for the LOT is $V_b$, for $L_b$ it is $V_{EW}$ and for the deflection coil it is $V_b$-$V_{EW}$. The scan voltage for the deflection coils can be changed by varying $V_{EW}$ with a constant $V_b$.

When the resonance frequencies of the separate tuned circuits are equal, there will be no interaction between the tuned circuits during flyback and the total flyback voltage will always be about 8 times $V_b$. In series with the horizontal deflection coil there is a (damped) linearity corrector coil. During the scan there is some loss in the resistance of the deflection coil. In the first part of a line the linearity corrector stores some energy in a permanent magnet until it is saturated. This improves the linearity of the horizontal scan speed.

The required S-correction for the picture tube can be adjusted with the value of Cs. The modulated S correction (inner pincushion correction) can be adjusted with the value of Csm.

In this receiver a special version of the diode modulator is used. With this implementation a linear horizontal zoom can be made without switching to different S correction capacitors. The principle is patented by Philips and fully described in application note AN96099.
All aspect ratio's can now be made via deflection control. For this 50Hz receiver 16:9, 14:9, 4:3 (or any other) applications can be made with either 4:3 or 16:9 picture tubes. The TDA8885 supports also a vertical scroll feature. This can be used to lift the zoomed picture, subtitling become visible again. The embedded software supports all these zoom features.

The modulating voltage $V_{EW}$ is obtained from the TDA8885 via an EW amplifier. The resistor $R_{EW}$ determines the amplification factor of the amplifier. $L_{EW}$ and $C_{EW}$ form a low-pass filter for the flyback pulses on the diode modulator so that on the E-W amplifier output only a field frequent voltage is present.

The voltages derived from the LOT are: EHT voltage, FOCUS, VG2, filament supply, +16V Vertical, +45V Vertical, +185V for video driver supply.

## 5.3 Vertical Deflection

The TDA8359 is a 9 pins vertical deflection circuit (3.2 $A_{pp}$) for DC-coupled 90° and 110° deflection systems with field frequencies from 25 up to 200 Hz. Two supply voltages are required, one supply voltage for the scan and a second supply for the flyback.

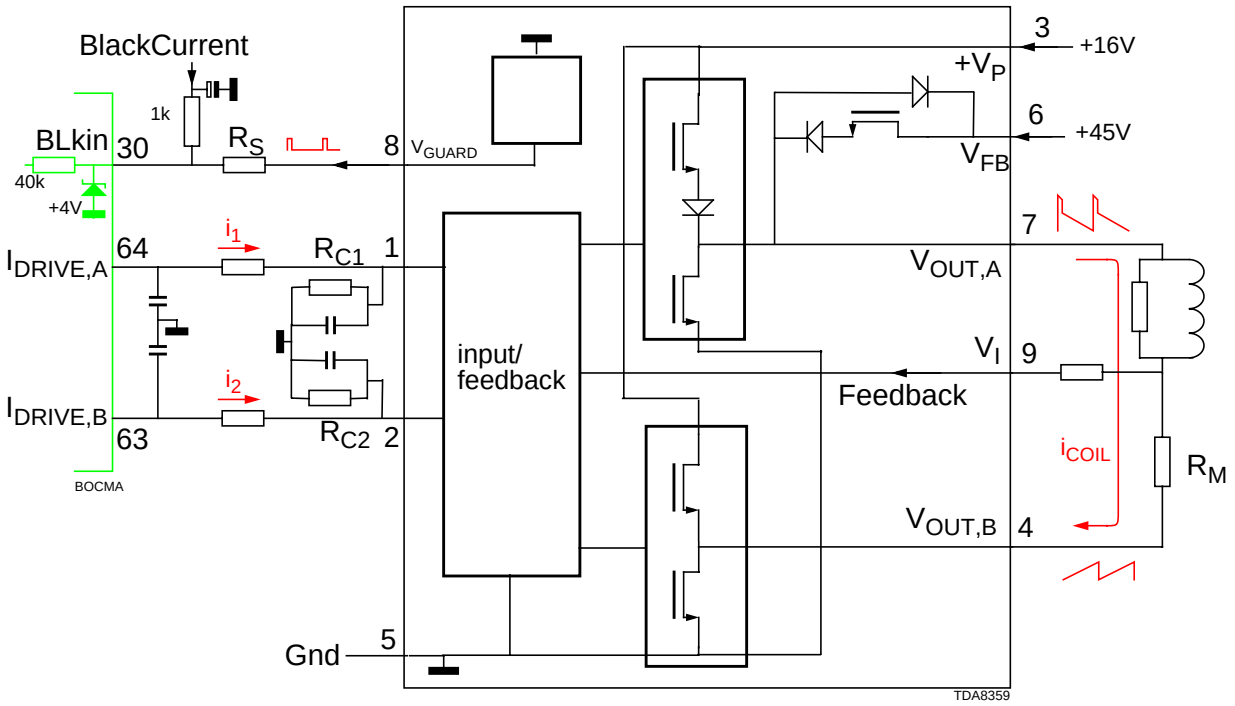



Fig.28 Block diagram of the vertical output stageTDA8359

The vertical drive currents of BOCMA pins 64and 63 are connected to input pins 1 and 2 of the TDA8359. The currents are converted to voltages via $R_{C1}$ and $R_{C2}$ . The differential input voltage is compared with the output current through the deflection coil, measured as a voltage across $R_M$, which provides the feedback

For HF loop stability a damping resistor (330 Ω) is added over the deflection coil.

The R-C filters at pin 63, 64 form a low-pass filter for better EMC immunity. The value of these resistors should be low in comparison to $R_{CON}$ (e.g. 100 Ohm), otherwise the maximum $V_{DRIVE}$ amplitude may not be reached.

A vertical guard pulse generated and can be used to protect the picture tube from burning-in during malfunctioning of the vertical deflection. During the vertical retrace the vertical guard output becomes high ($U_{vguard}$ = 5.0 Volt at $I_{vguard}$ = 500 uA for about 1mSec time period). This is sensed by the BOCMA BLKin input pin 30 (combined Vguard +BlackCurrent). The condition can be read via bit **NDF**. To protect the picture tube against burn-in, the $RGB_{OUT}$ pins will be blanked (when protection enabled by **EVG** = 1).

# 6. Software

This application note is based on the lmrdtv_3.0 release of the LMR-DTV software.

The use of the TV is not changed for analogue channels. Digital channels are also handled as analogue channels, only the installation of a digital channel is different (see chapter installation of channels). When a digital channel is selected the frequency and the pid values of the program must be known and programmed.

The concept of the CTV software is still the same. On how to use the system see [2].

## 6.1 Install Menu

The installation menu consist of the following items:

- Prog. Nr
- System
- Frequency
- AFC
- Fine Tune
- Dig Channel
- PCR PID
- VID PID
- AUD PID
- Name
- Store
- Autostore

The installation menu can be reached by pressing the menu button, and select the item installation. A new menu pops up in which again the installation item must be selected.

### 6.1.1 Prog. Nr

With this item the program number can be changed. The TV will tune to this program and the menu is updated with the settings of this program. The program number can be changed with cursor left/right keys or by entering a digit with the digit keys.

### 6.1.2 System

Selects the colour system of the selected channel. A selection can be made with the cursor left/right keys.

### 6.1.3 Frequency

Displays the frequency of the current tuned channel. In this menu item a new frequency can be entered with the digit keys. With cursor left/right the frequency can be changed with steps of 0.25Mhz. When the frequency is changed the new frequency is directly written to the tuner.

### 6.1.4 AFC

Turns the automatic frequency control on or off. When the channel is a digital channel the AFC is turned off.

### 6.1.5 Fine Tune

With cursor left/right the frequency can be adjust with steps of.25Mhz. When this is used the AFC is switched off automatically.

### 6.1.6 Dig Chan

This item indicates whether the program is a digital channel or not. When a digital channel is selected the AFC is turned off automatically.

### 6.1.7 PCR PID

The pcr pid can be programmed with this item. The pid value can be entered by the digit keys. With cursor left/right the value can be changed with steps of 1. When the pid value is changed or entered it is directly made active. The value must be entered, and is displayed in decimal. The value of the pid must be between 0 and 8191 (0x1FFF).

### 6.1.8 VID PID

The video pid can be programmed with this item. The pid value can be entered by the digit keys. With cursor left/right the value can be changed with steps of 1. When the pid value is changed or entered it is directly made active. The value must be entered, and is displayed in decimal. The value of the pid must be between 0 and 8191 (0x1FFF).

### 6.1.9 AUD PID

The audio pid can be programmed with this item. The pid value can be entered by the digits keys. With cursor left/right the value can be changed with steps of 1. When the pid value is changed or entered it is directly made active. The value must be entered, and is displayed in decimal. The value of the pid must be between 0 and 8191 (0x1FFF).

### 6.1.10 Name

With this entry the selected program can be given a name by the user. With cursor left and right the first, second etc. characters of the name can be selected. If a character is selected the character can be changed with the cursor up/down keys.

The changed name is directly written to the non-volatile memory.

### 6.1.11 Store

This menu item is activated with the cursor left and right button. It stores the frequency, AFC, digital channel, PCR PID, VID PID and AUD PID for the selected channel in the non volatile memory of the analogue board.

### 6.1.12 Autostore

This function scans the whole frequency band and searches for programs and stores them after each other beginning with the program number from which it is started up. The autostore function only finds analogue channels. So no digital channels are found during auto search.

## 6.2 Analogue keys

All the keys have the same function as in the CTV demo software (see [2]).

New keys:

subtitle key: Toggles the TV between normal operation mode and digital demo mode. The functionality of each key in digital demo mode is described in paragraph Digital demo mode keys.

## 6.3 Digital demo mode keys

stb-key Resets the digital board. The TV goes out of digital demo mode back to normal operation mode.

menu-key Toggles the main menu of the digital demo menu (see Digital Menu's) on and off.

mute-key Toggles the mute on the digital board.

vol-up Volume up on the digital board.

vol-down Volume down on the digital board.

## 6.4 Digital Menu's

### 6.4.1 General Menu navigation

With the cursor buttons (left, right, up and down) the different menu items can be selected.

A selected menu item can be activated with the pp-button. If the selected item is a sub-menu this menu will be entered, if it is
a selection box the next selection will be selected and when the item is a number box, digits can be entered or with cursor left/right the value can be changed.

### 6.4.2 Main menu

The main menu contains the following items:

- Installation menu (See Installation Menu)
- Feature menu (See Feature Menu)

### 6.4.3 Installation Menu

This menu contains the following

- Channel With this item is selected whether the cable or the COFD (terrestial) demodulator is used.
- OSD Compensate the OSD delay for the analogue channel. This item is used to put the OSD for an analogue channel on the same place as for a digital channel.

### 6.4.4 Feature Menu

This menu contains the following items:

- Graphics
- Scaling
- Video

These are all submenu's which are described below.

#### 6.4.4.1 Graphics

This menu contains the following menu items:

- Drawing menu — Displays a bit map on the screen with various filled and non-filled shapes, together with text rendered in different fonts.
- Tiling menu — This is a demonstration of the 7215's hardware tiling feature. After selecting the Tiling Demonstration, select Start: The cursor keys can now be used to select an area to be tiled. Select the start position by pressing PP then move the cursor again to create the area you wish to tile; press PP to confirm the selection. Unfortunately the cursor is not visible so it is not possible to see the selected area.The selected area is tiled with the philips logo.
- Fast transfer — Demo shows a 3D effect Philips logo rotating in the centre of the screen. This demonstrates the 7215's ability to rapidly update a bitmap displayed on the screen.
- Hard wipe — The hard wipe demonstration shows overlapping sub-regions within the same graphics plane. After selecting the Start button, the user can select one of the two bitmaps using the cursor keys and the PP button. The selected bitmap will appear at the top of the display stack and can be moved around using the cursor keys. Bitmap selection can be toggled using the "yellow" key on the remote control handset. Pressing the PP key again returns to the Hard Wipe entry screen.
- Soft wipe — The soft wipe demonstration shows two bitmaps, displayed on separate graphics planes, allowing both overlapping and transparency between bitmaps. After selecting the start button, the user can select one of the two bitmaps using the cursor keys and the PP button. The selected bitmap will appear at the top of the display stack and can be moved around using the cursor keys. The selected bitmap can be toggled using the "yellow" key on the remote control handset. Pressing the PP key again returns to the Soft Wipe entry screen.
- Planes — The planes demo shows the different graphics planes available on the SAA7215. When the planes demo is selected, a scene showing all five planes is displayed. The scene is composed as follows: Background plane, Video plane (scaled to quarter screen, top left of picture), Graphics Plane 1 (BMP picture, bottom right of picture), Graphics Plane 2 (menu graphics), Cursor Plane.
- Fade — To demonstrate the different transparency levels supported by the 7215 graphics hardware, the Fade Demo displays a bitmap over video while continuously varying the bitmap transparency. This gives the effect of continuously fading the bitmap in and out. This fading in not visible in our case because the picture is blanked so the normal video is not shown in the back ground.

#### 6.4.4.2 Scaling

Do not use.

#### 6.4.4.3 Video

The demonstration gives the user control of SCAN, FREEZE, PLAY and STOP features.

| | |
|---|---|
| Scan | Displays I Frame only (for use with display of fast forward from storage media) |
| Freeze | Freezes the display on the current frame |
| Stop | Stops all video playing |
| Play | Starts video playing after a SCAN, FREEZE or STOP. |

## 6.5 Known problems

1) Sometimes a line of the start-up Philips logo disappears.
2) Philips logo is sometimes displayed bigger after a channel change which results that the last one or two lines of the OSD are not displayed any more.
3) Sometimes a character stays on the screen.
7) When pressing the status key a channel logo is displayed for a very short time and it is replaced by --/-- (time indication).
10) In the volumebar a pixel is lost at the most right vertical border line when the volume is at its (maximum -1) or (maximum -2).
12) Menu is sometimes removed in a strange way. When the menu is removed it is shifted to the right. Normally all the lines are shifted all together so the menu is still a square. Sometime this square is somewhere broken in the middle and shifted a few pixels.
16) TXT-picture is shifted.In the hardware there are registers with which the TXT picture can be shifted but it is not possible with the current txt-library to access these registers.
18) When the halt-key in TXTmode is pressed a wrong character is displayed at the top left of the teletext screen.
24) It is not possible to store PP.
25) When the colour system of the menu is put on auto, the menu starts to flicker because of the continues updates of the menu.
26) When the fine-tune bar is completely at the right or left it suddenly jumps back to the middle of the bar. This looks weird.

29) It takes a long time before a noise channel is tuned and unblanked. This can result that the channel is skipped during zapping (pressing the channel-up/down key continuously).

30) Cursor only half visible at the edges of the menu.

    Can not be solved till we have real fast blanking. At the moment we only activate the graphics (fast blanking) pin for the menu.

31) Some lines in the digital menu's are shifted or doubled.

    This is probably a problem of the draw scan line function.

32) gfx-box's (fast blanking line) does not always fit the OSD box

34) When a digital menu is drawn a black square is visible before the OSD is visible. This is because the fast blanking is active before the OSD is drawn.

39) The scaling menu is not made visible (this is probably because the fast-blanking is not made active for this menu)

41) Sometimes an unstable channel logo is made visible (the OSD is walking over the middle of the screen) when there is a channel change from a digital to an analogue program. It seems that the digital part is not in slave mode yet.

42) Sometimes when a digital channel is tuned the channel logo displays the wrong program number (if it is wrong it always displays channel 0 while it is tuned to the right channel)

49) Channel logo is not always removed after 5 seconds. If it is not removed it stays on the screen till another channel change.

51) It is not possible to show the cursor only on RGB. WORKAROUND. The cursor is shown on RGB and Y/C but on Y/C the cursor is made transparent so the user does not see this.

54) There is some colour difference in the cursor when the cursor is displayed at the left or at the right of the screen

57) Sometimes the analogue sw seems to resets itself.

59) For some demo's like hardwipe, video must be visible at the back ground. This is not the case at the moment. With this fast-blanking (gfx-pin) solution it is not possible to solve this. With another fast blanking solution this is perhaps possible.

62) When an extension (AV1 of AV2) is chosen and a digit key is used to return to front end, a wrong program number is displayed

63) It is not possible to store the digital installation information (pids) of the higher programs. It seems that it is only possible to access 1k of the NVM of the analogue board.

64) AV2S (and AV3S without digital add-on) selection is not supported by the software.

65) AV status detection is not supported by the software.

# 7. EMC

## 7.1 General Aspects

In this chapter the EMC design considerations are described. The EMC results of the entire receiver are not all measured yet.

For this hybrid type receiver, where a rather immune but radiating digital part is combined with a sensitive analogue signal processing part, EMC aspects are very important.
Another fact is that in Europe a TV receiver must have the CE product mark which implies that the set is compliant to the European EMC rules for immunity but also within the limits of radiated energy!
The application of the digital MPEG source decoding part in a TV receiver is quite different from the conventional setup of a digital satellite set-top box which is always shielded. The design goal is to prevent that a full metal shielding of the digital part is needed.
With this background the chosen component and board setup can be explained.

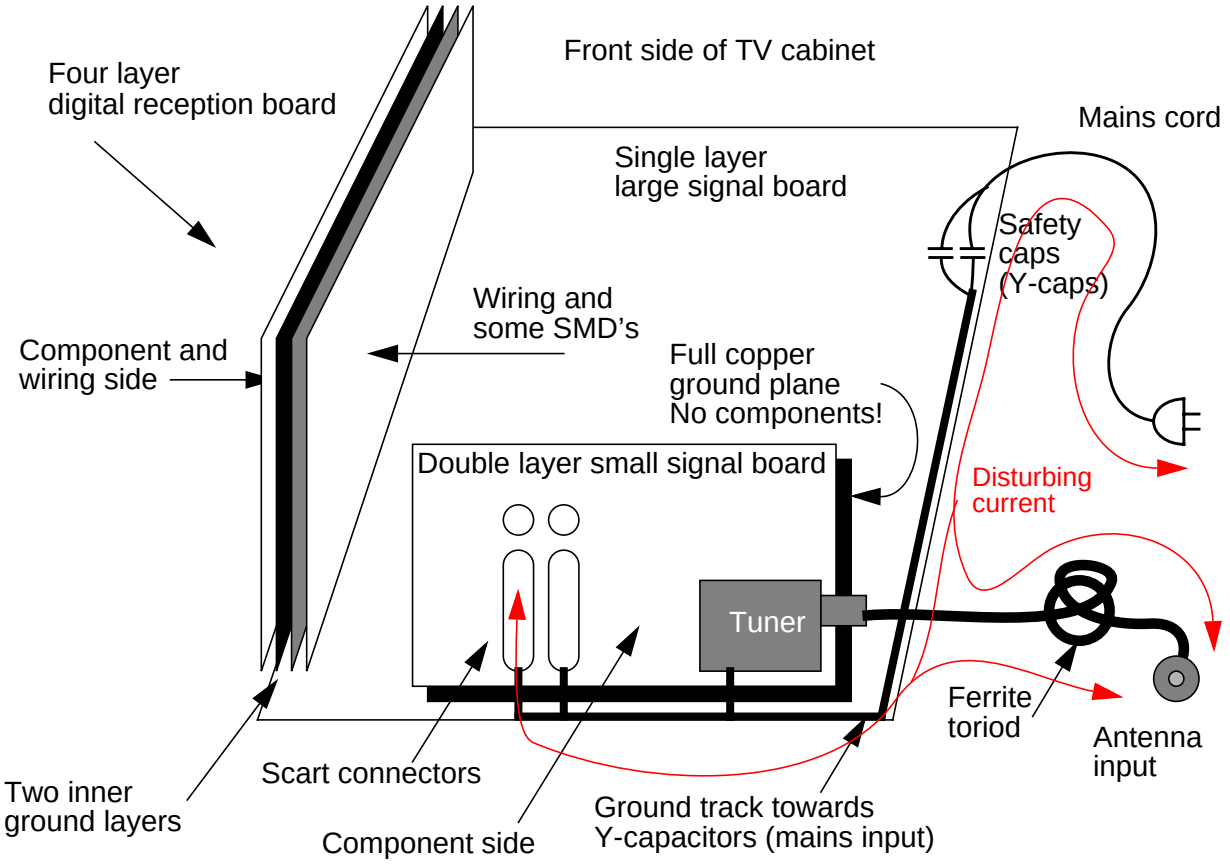



Fig.29 Component and board setup in relation with EMC

The tuner is placed at the position where it has the shortest connection, via a thick ground track on the large signal board, towards the safety capacitors (also called Y-caps). Now, when the injected current immunity test on tuner input is measured, the injected disturbing ground current will NOT flow through the small signal board, but is routed to the mains cord where it will be absorbed by the mains input circuitry (two times 150Ω as defined in EN55020).

This situation is the same for the injected current immunity test on mains input. The only difference is that the current is injected at mains input, and absorbed by the load resistor on the tuner ground.

The advantage of placing the tuner and the IF circuitry at the chosen position is that it is far from the digital part. Now when the radiation is measured, the risc that the disturbing spectra from mainly the transport stream bus (like the common interface cable!), is coupled to the tuner ground, where it is measured in the radiated EMC test.
For open antenna reception, like it is planned for DVB-T in some european countries, the tuner ground must be free of any disturbances generated by the digital part. Some measurements of tuner ground currents indicated that the harmonics of the used symbol frequency in the transport stream, together with the used MIPS clock frequency, can easily fill the spectrum up to 500MHz at a level of a few hundred micro volts!

## 7.2 Analogue Reception part

The small signal analogue reception board is made with a double layer PCB. To prevent magnetic coupling between the large and the small signal part, one layer is a full copper plane.

Although this choice leads to more board space, it was chosen to minimise the risc of self-pollution. In a later phase, the experiment with a single layer small signal board is now very simple, just leave out the second fulll copper layer and add ground tracks on the remaining layer. The design rules for a single layer small signal application are described in application note AN98097.

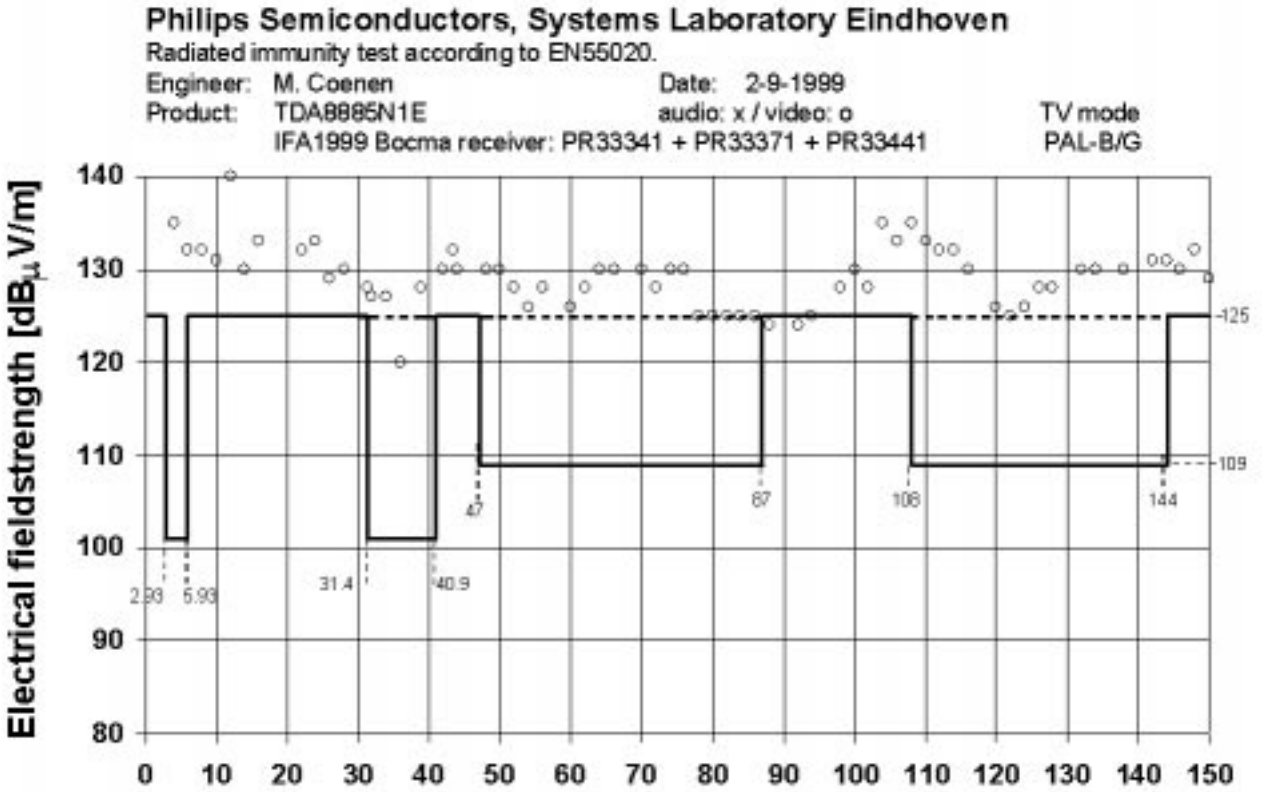



Fig.30 Radiated Immunity (Jacky test) of Analogue Reception Part

The measured radiated immunity, as shown in the diagram, is dominated by vertical deflection disturbances. Only in the frequency range between 31.4 and 40.9MHz, the IF range, other picture

disturbances are visible. The two times IF disturbances at 77.8MHz can not be seen anymore. The colour disturbances at three times IF, 116.7 + 4.433 and 116.7 - 4.433 are just more visible than the vertical modulation. IF + 4.433 -43.33 is above the limit.
The vertical disturbances are picked-up by the RGB cable between CRT panel and the small signal board. It must be prevented that these disturbing current from the CRT cable enters the TDA8885 via its RGB outputs. This can be done by placing three small (20pF) capacitors at the RGB connector (on the small signal board) and connect them to the ground plane. Now the moment the RGB cable enters the small signal board, the disturbing high frequency current is routed to the ground plane. Under this condition the radiated immunity is measured.
A further overall improvement for this vertical disturbances (at least +5dB from 50 to 150MHz) can be made by using a ferrite toroide in the RGB cable.

All peripheral in- and outputs are filtered. The video signals are switched in the BOCMA and the sound signals are switched in the TDA9875. The peri's are placed in between these IC's, now the track lenght between peri in/outputs and the IC's are very short. When these peri in/output tracks, during the EMC immunity tests, are polluted, it is prefered that the return ground current will follow the track in the copper back layer (as the mirror current right beneath the track). In this way the disturbing ground current remains local and is not routed to other sensitive circuitry. For this reason it is important that the ground path from the peri connectors to the large signal board does not cross other circuitry. To improve this ground plane effect, the thickness of the board is reduced from the normal 1.6mm to 1.2mm.

The peri connectors on the small signal board are the separation between the analogue signal processing part (the right hand part where BOCMA, tuner and IF is located) and the digital processing part, TV controller and digital sound. These not sensitive devices are close to the digital board.

## 7.3 Digital Reception Part

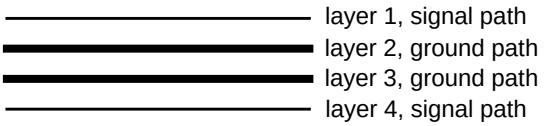



Fig.31 Layer usage on digital board

This layout structure is different from the conventional four layer setup were the inner layers are one ground plane and a power supply plane. The advantage of two identical inner ground planes is that the coupling of both outher wiring planes to the inner ground planes is identical. This balanced structure has a more predictable HF behaviour. The routing of track is not so critical.
Signal layer 1 is located on the left hand side of the chassis (observed from the rear side). On this layer the IC's are mounted. The magnetic radiation of the IC's can not couple to the small signal board which is located at the other side. The higly radiated transport stream bus is also routed on signal layer 1.
Signal layer 4 contains only some SMD components.
By exception, sometimes layer 3 is used to make some jumps for the power supply tracks.

The TDA8048H has the following supplies and groundings: Vdd (core and pads), VddAnalogue, VddDigital and VddCLock. Every supply has its own track with inductor and decoupling capacitor.

The SAA7214 has the following supplies and groundings: VddCore, VddPerifery and Vdd_PLL and its corresponding grounds. Each supply should have its owns supply track with inductor and decoupling

capacitor; except VddCore, because decoupling is done internally in the IC (an external capacitor can even worsen the radiation). For experiments the VddCore capacitors can still be mounted.

This is also for the SAA7215, there are the supplies: VddCore, Vdd and VddAnalogue. There is should be the same. The supplies of the used SDRAMS are connected to the Vdd supplies of the SAA7215.

The memories have there own supply.

To filter high frequencies currents, every power supply has a BLM21A102S series coil. These type of coils have a high impedance even at high frequencies (due to their very low capacitance, Rdc=0.45Ω, Imax=200mA).

The filter in the DIF part is placed in such way that the first part of the filter is placed as close as possible to the connector and the last part, an RC network, is placed close to the vicinity of the TDA8048H. Disturbances which are picked up via the track are filtered near the TDA8048H and don't enter the TDA8048H.

The filters which are used at the analogue Y, C and RGB are also placed at the vicinity of the connectors. These low pass filters consists of a first order RC filter and a second order RCL filter.

In the digital to analogue connector every signal has an impedance in its path, a BLM21A102S coil or a 100Ω resistor.

## 8. Abbreviations

| | |
|---|---|
| AC-3 | Audio Coding |
| ADC | Analogue Digital Converter |
| AFC | Automatic Frequency Control |
| AGC | Automatic Gain Control |
| AM | Amplitude Modulation |
| AV | Audio Video |
| AVGD | Audio Video Graphics Denc=(Digital encoder) |
| BOCMA | Bimos One Chip tv-ic for Mid-end Application |
| BTSC | Broadcast television System Committee |
| CCC | Continuous Cathode calibration |
| CTI | Colour Transient Improvement |
| CI | Common Interface |
| COFDM | Coded Orthogonal Frequency Division Multiplexing |
| CVBS | Composite Video Baseband Signal |
| DIF | Digital Intermediate Frequency |
| DRAM | Dynamic Random Access Memory |
| DSP | Digital Sound Processor |
| DVB | Digital Video Broadcasting |
| DVB-C | Digital Video broadcasting-Cable |
| DVB-T | Digital Video Broadcasting-Terrestrial |
| DVD | Digital Versatile Disk |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| EHT | Extra High Tension |
| EPROM | Electrical PROM |
| EMC | Electro Magnetic Compatibility |
| EW | East West |
| FM | frequency Modulation |
| fs | sample rate frequency |
| IC | Integrated Circuit |
| IF | Intermediate Frequency |
| IIC | Inter Integrated Circuits |
| IIS | Inter Integrated Sound |
| IFA | International Funkt Aufstellung |
| I/O | Input/Output |
| IRQ | Interrupt ReQuest |
| LED | Light Emitting Diode |
| LMR-DTV | Low Mid-Range Digital Television |
| LOT | Line Output Transformer |
| LPF | Low Pass Filter |
| LVDMOS | Low Voltage Depletion Metal Oxide Semiconductor |
| MIPS | Microprocessor without Interlocking Pipeline Stages |
| MPEG | Motion Picture Experts Group |
| NICAM | Near Instantaneous Companded Audio Multiplexing |
| NTSC | National Television Standard Committee |

| | |
|---|---|
| OSD | On Screen Display |
| OTP | One Time Programmable |
| PAL | Phase Alternating Line |
| PCB | Printed Circuit Board |
| PCMCIA | Personal Computer Memory Card International Association |
| PCR | Program Clock Reference |
| PES | Packized Elementry Stream |
| PID | Packet IDentifier |
| PIP | Picture In Picture |
| PLCC | Plastic Leaded Chip Carrier |
| PLL | Phase Locked Loop |
| PMT | Program Map Tables |
| PP | Personal Preferences |
| QAM | Quadrature Amplitude Modulation |
| QFP | Quad Flat Package |
| QSS | Quasi Split Sound |
| RC5 | Remote Control code 5 |
| RGB-Fbl | Red Green Blue_Fastblanking |
| RS | Reed-Solomon |
| SAW | Surface Acoustic Wave filter |
| SCART | Syndicat des Constructeurs d'Appareils de Radio et Television |
| SDRAM | Synchronous DRAM |
| SECAM | Sequentiel Couleur A Memoire |
| SIF | Sound Intermediate Frequency |
| SLE | Systems Laboratory Eindhoven |
| SMD | Surface Mounted Device |
| SMPS | Switched Mode Power Supply |
| SPDIF | Sony/Philips Digital Interface |
| S-VHS | Super Video Home System |
| TOP | Take Over Point |
| TS | Transport Stream |
| TV | TeleVision |
| UART | Universal Asynchronous receiver Transmitter |
| VCXO | Voltage Controlled Crystal Oscillator |
| Y/C | Luminance / Chroma signal |
| YUV | Luminance signal, U Colour difference signal -(B-Y), V colour difference signal -(R-Y) |

## 9. References

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[ 4 ] AN98051, GTV1000 Global TV Receiver

[ 5 ] AN98092, The GTV2000 Demo Receiver

[ 6 ] AN98101, PR31901 Compact 90 degree TV receiver with TDA935x/6x/8x Ultimate One Chip

[ 7 ] AN98011, 200W SMPS with TEA1504

[ 8 ] AN96099, Diode modulator for linear zoom

[ 9 ] AN98097, EMC guidelines for TDA88xx applications

[ 10 ] VLSI/ComAtlas AN9600-1, Fast scanning with the VES9600

[ 11 ] VLSI/ComAtlas CAS2596A DVB-T Front-end board